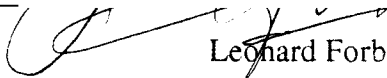


AN ABSTRACT OF THE THESIS OF

Jing Zhang for the degree of Master of Science in Electrical and Computer Engineering
presented on November 27, 1995. Title: Generation of Substrate Bias and Current
Sources in CMOS Technology.

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Abstract approved: _____


Leonard Forbes

A negatively biased substrate has several advantages over a grounded substrate in CMOS technology. The on-chip generation of this negative substrate bias has made chips easier to use when only a single supply is preferred. This project demonstrates two types of charge pump circuits used to generate negative voltages not only for biasing the substrate, but in a broader sense also for other purposes in CMOS technology. One other possible use is in conjunction with 'Guard Ring Diodes for Suppressing the Substrate Noise in Mixed-Mode CMOS Circuits'. This work proposes a reasonable approach to generate the forward biasing current for the guard ring diode whose depletion capacitance and the substrate lead inductance form a resonant circuit to provide very low substrate-to-ground impedance at specific frequencies. Given this emphasis on generating a reasonably predictable current source, the generated negative voltages are regulated using a feedback loop. The amplitude of this negative voltage can be determined exclusively by transistor sizes.

Simulation results support the theoretical analysis in that accurate negative voltages and current sources can be generated on-chip, although there are some limitations.

Generation of Substrate Bias and Current Sources in CMOS Technology

by

Jing Zhang

A THESIS

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

Presented November 27, 1995

Commencement June 1996

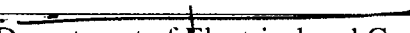
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
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Acknowledgments

I would like to thank all the people who helped me with their advice during the realization of this thesis project.

In particular I want to thank:

My major professor Leonard Forbes who sparked my interest in this new field of mixed-mode integrated circuits and advised me through the sometimes difficult realization. My wife, Ling, whose encouragement and endless patience made the completion of this work possible. My fellow engineer Bruce Savage at Flight Dynamics who carefully reviewed the manuscript and gave me many valuable suggestions. My friend Mrs. Ruth who took time to polish my English writing.

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GENERATION OF SUBSTRATE BIAS AND CURRENT SOURCES IN CMOS TECHNOLOGY

1. INTRODUCTION

The use of negative substrate bias voltage V_{BB} has several advantages over a grounded substrate. It lowers the sensitivity of threshold voltages to the body effect, increases punch-through voltages, lowers the diffusion-to-substrate capacitance without requiring a decrease in substrate doping, and increases the gain of typical inverters. It also lowers subthreshold leakage on clocked depletion transistors and protects the chip against forward-biasing of the substrate due to voltage undershoots at the inputs, which are common with TTL peripherals. If feed back is provided, V_{BB} voltage can compensate for some device parameter variations [2].

As applied in particular to DRAM circuits, back bias greatly reduces the probability of localized forward biasing of junctions. Such forward biasing injects electrons into the substrates and can lead to a malfunction of dynamic circuits or seriously reduce refresh times. This is because the electrons will be collected in the “potential wells” beneath the capacitor plate for stored “ones”. Another advantage is that speed and power both tend to improve with back bias. This is because transistors operate in the flatter portion of the body-effect curve and lose less drive capability as their sources rise, and because the lower junction capacitance reduces the load [3].

Substrate noise is a serious concern and limitation in mixed-mode, analog-digital, CMOS integrated circuits. The use of forward-biased n+-p guard ring diodes which resonate with the substrate lead inductance is demonstrated by simulations to be effective in reducing this substrate noise by an order of a magnitude. The basic idea is

to create a band pass filter whose frequency response is decided by the inductance of the bond wire and the capacitance of the forward biased diode. Because the capacitance of the guard ring diode is proportional to the biasing current, the frequency of the filter can be adjusted by changing the current through the diode [4]. Detailed work on guard ring diodes for suppressing the substrate noise in mixed-mode CMOS circuits can be found in separate papers. Generally the required biasing current is within the range of 2-20 μ A.

This paper will focus on the on-chip generation of negative substrate bias and current sources for the guard ring diodes in CMOS technology.

2. REVIEW

Widely used in DRAM chips, the on-chip generation of negative substrate bias has been an important part of the DRAM technology. DRAM's generally require one positive supply, one negative supply, and ground. The negative supply is required for substrate biasing largely to prevent substrate injection currents that can cause a loss of stored charge in dynamic memory cells.

To make chips easier to use while applying the back bias, only single positive power supply is preferred. Self-biased technique can eliminate the use of externally provided back bias voltages [3][5]. Various works and publications on negative voltage generators using a single positive supply have been seen in the past two or three decades. Most of the circuits are based on charge pump theory.

Lance A. Glasser & Daniel W. Dobberpuhl [2] described in detail the operation theory of free-run charge pump circuits for generating on-chip negative substrate biases. The theoretical minimum voltage that can be generated is about $-V_{DD}$ plus two diode drops.

Often a regulated and controllable V_{BB} is more desirable because of chip to chip variation. William L. Martino et al. [3] report that through feedback loop regulation, a known regulated on-chip back bias voltage can be generated in NMOS technology. In CMOS technology a similar control scheme can also be implemented in order to produce this bias voltage which is predictable and regulated.

Based on the basic charge pump theory, various configurations have been seen for different applications. Seung-Moon Yoo et al. [6] and Hiroo Masuda et al. [7] report interesting circuit configurations to generate substrate biases for DRAM circuits.

As the DRAM technology advances rapidly, to reduce power dissipation and improve device reliability, the operating voltage of high-density DRAM's is expected to be reduced greatly but the back biases need to be at about -1.5V. This triggered the research of generating on-chip back biases with supply voltages reduced to as low as 1.5V. Yasuhiko Tsukikawa et al. [8][9] proposed the hybrid pumping circuit to overcome the shortcomings of conventional back bias voltage generators which can only generate a minimum voltage of $-V_{DD}$ plus 2 diode drops.

In conjunction with 'Resonant Forward-Biased Guard Ring Diodes for Suppression of Substrate Noise in Mixed-Mode CMOS Circuits' project [4], a known biasing current for the guard ring diodes can be generated using a current sink or source [10].

Normally the substrate is biased at about -1V to -1.5V. For the guard ring diode biasing, the cathode of the guard ring diode should be at a even more negative voltage in order to forward bias the diode. No previous work has been seen in generating current sources for this particular application.

3. CHARGE PUMP THEORY

A negative voltage can be generated by pumping electrons out of the ground node and into the substrate. Because substrate is a giant capacitor (on the order of 1000pf), this slowly lowers its voltage. A conceptual V_{BB} generator configuration is shown in Figure 1.

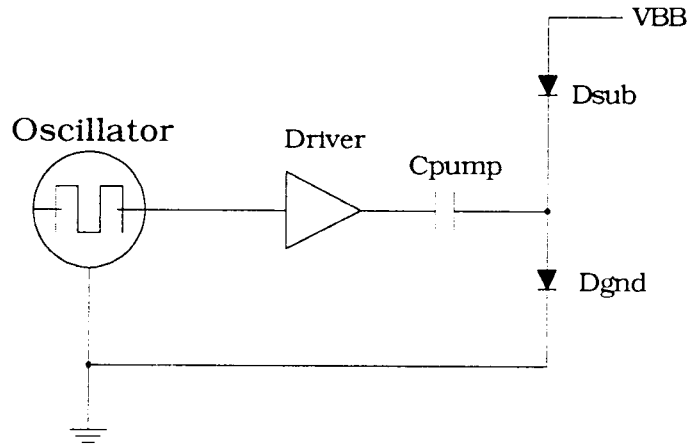


Figure 1. Concept of Charge Pump V_{BB} Generator

The driver amplifies the ac signal generated by the oscillator and powers the charge pump. The power is coupled through the capacitor C_{pump} . The two diodes D_{gnd} and D_{sub} gate the charge out of the substrate and into the ground node. When the voltage V_{pump} is near its peak value, then D_{gnd} is forward biased and charge is being pumped into the ground node. The other diode D_{sub} is off. On the other half of the cycle, V_{pump} is near its most negative value and D_{gnd} is off, while D_{sub} drains charge out of the substrate. Obviously, charge does not flow across the capacitor [2].

3.1 The Oscillator

The oscillator can be a ring oscillator or a Schmitt trigger. For a N stage ring oscillator, where N is an odd number, the oscillator frequency f is approximately $(2N\tau_{\text{delay}})^{-1}$, where τ_{delay} is the delay of a single stage. This relation is only approximate because the loading on all stages is not equal. Also N should be greater or equal to 5; otherwise the voltage swing may be too small. Figure 2 shows the circuit of a 7-stage ring oscillator.

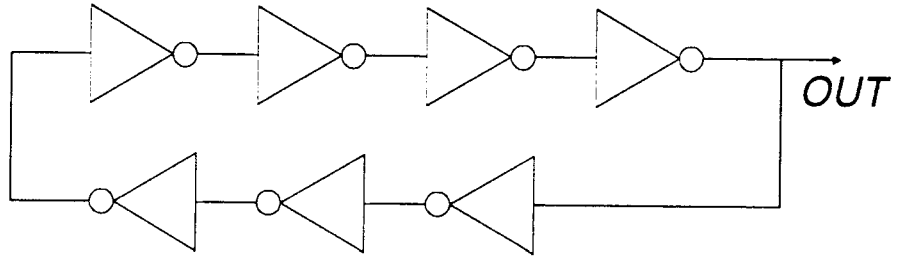


Figure 2. 7-Stage Ring Oscillator

3.2 The Charge Pump Diodes

The theoretical minimum value of V_{negative} is determined by the peak-peak value of V_{pump} and voltage drops on the two diodes. During the high part of the cycle, V_{pump} must be one diode drop (diode D_{gnd}) above ground to pump charge. On the low side of the cycle, V_{pump} must be a diode drop (diode D_{sub}) below V_{BB} to do any work. Assuming the maximum peak-to-peak voltage of V_{pump} is less than V_{DD} , then the minimum V_{BB} is greater than or equal to $-V_{\text{DD}}$ plus two diode drops. Because of leakage currents and parasitic capacitances, the actual value should be lower than this ideal one [2].

The diode D_{sub} may be implemented as a p-n diode naturally provided by the CMOS technology. The diode D_{gnd} may be a p-active sitting in a grounded n-well or a n-transistor configured as a diode.

If the diodes are ideal, the current pumped out of the substrate would be:

$$I_{\text{avg}} \approx C_{\text{pump}} \Delta V f \quad (1)$$

where ΔV is the difference between the substrate voltage V_{BB} and its theoretical minimum value of V_{BBmin} . The current is large when ΔV is large--that is, when the pump first starts up. The pump must work at all V_{BB} voltages between zero and its minimum value. I_{avg} increases with the pumping rate f . Obviously the I_{avg} and V_{BB} ideally have a linear relationship.

Equation (1) is valid when all of the charge represented by $\Delta V C_{\text{pump}}$ is actually pumped out of the substrate. This is always true for ideal diodes, but for real devices the finite resistance of the forward-biased device severely limits the effectiveness of the charge pump. The principal question is whether the RC constant of the diodes and pump capacitor is larger or smaller than $1/f$. If the time constant is short (ideal diodes), equation (1) prevails and the V_{pump} wave form is clipped. If the time constant is long, V_{pump} is roughly sinusoidal.

3.3 The Coupling Capacitor

The coupling capacitor transfers power from the driver into the charge pump, where it does the work of moving electrons from a higher potential to a lower one.

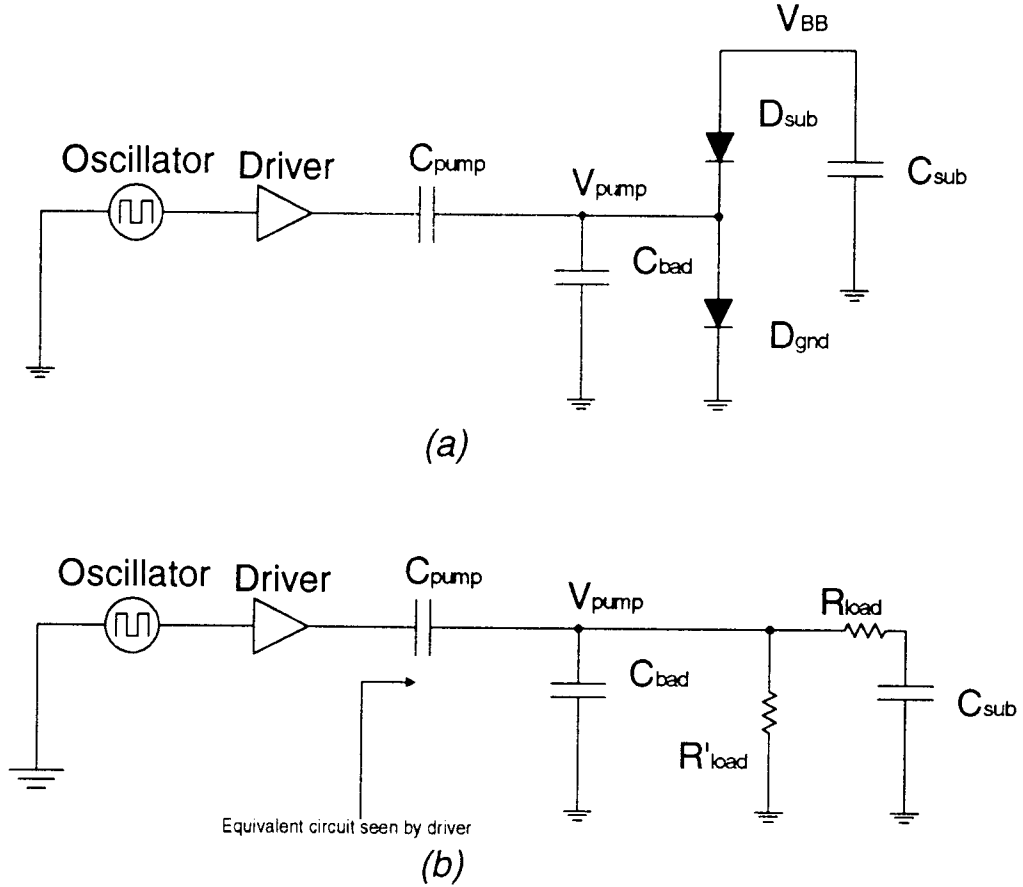


Figure 3. Models of V_{BB} Generator Showing (a) Important Capacitances (b) Small Signal Model

Figure 3 illustrates a V_{BB} generator with important capacitors explicitly denoted. C_{bad} is a parasitic capacitor that acts to lower V_{pump} and hence the minimum value of V_{BB} . C_{bad} is mostly from the diode capacitances. Because $C_{sub} \gg C_{bad}$ and $G_{load} \ll 2\pi f C_{pump}$ when $V_{BB} \approx V_{BBmin}$, we have

$$V_{pump} \approx \frac{C_{pump}}{C_{pump} + C_{bad}} V_{drive} + V_{offset} \quad (2)$$

If the peak-to-peak voltage of V_{drive} is V_{DD} , we then have

$$V_{\text{pump-p}} \approx \frac{C_{\text{pump}}}{C_{\text{pump}} + C_{\text{bad}}} V_{DD} \quad (3)$$

If we want to achieve lowest V_{BB} possible, clearly we have to minimize C_{bad} so as to decrease $V_{BB\text{min}}$. To make $V_{\text{pump-p}}$ large, we require $C_{\text{pump}} \gg C_{\text{bad}}$ and $G_{\text{load}} \ll 2\pi f C_{\text{pump}}$. To minimize C_{bad} , we want to lay out C_{pump} as a large square P transistor with the source and drain connected.

Assuming the gate is connected to the charge pump, a N transistor would clearly have a problem in that the p-n junction of body-source(drain) can be forward-biased, since the substrate voltage could be momentarily higher than the V_{pump} by the voltage of one diode drop. Also the channel disappears most of the time if the source-drain is connected to the charge pump. Ideally we want the P transistor's source-drain to be connected to the charge pump so that the transistor is mostly in linear mode and the channel is present almost all of the time. This way we can always have a relatively stable C_{pump} as

$$C_{\text{pump}} = C_{gs} + C_{gd} = w/l C_{ox} + C_{\text{fringing}} \quad (4)$$

3.4 The Driver

Fortunately, from Figure 3 we observe that the driver does not need to drive an equivalent load of C_{pump} . The driver should be swinging from rail to rail when $\Delta V \approx 0$.

Under these conditions, the R_{load} is very large and the equivalent load of the driver is C_{pump} in series with C_{bad} , or approximately C_{bad} .

In the steady state, the average current I_{avg} pumped by the bias generator equals the leakage current into the substrate. This leakage is caused primarily by minority carrier injection into the substrate from saturated load devices (hot electron effects). A typical leakage current is around $5\mu\text{A}$.

4. CIRCUITS AND SIMULATIONS

4.1 Free Run Charge Pump Circuits

4.1.1 Negative Voltage Generator

First we will investigate the basic free-run circuit. From the basic pumping circuit described above, we will analyze the requirements for the ring oscillator, driver, charge pump capacitor, charge pump diodes, and the loading conditions.

Figure 4 is the complete schematic of basic free-run charge pump circuit for V_{BB} generation. The ring oscillator being used is a 7-stage CMOS inverter chain. The driver following the inverter is configured as two inverters in a row where the sizes can be adjusted to provide sufficient current, and if larger charge current is needed the number of inverters can be easily increased. The P transistor with drain and source connected served as the charge pump capacitor where the dimension of the transistor is approximately proportional to the equivalent capacitance.

Referring to equation (1), the pumping current is proportional to the ring oscillator frequency, the charge pump capacitor, and the voltage difference between ideal minimum voltage and actual output voltage. Meanwhile, the driver should be able to provide sufficient current to charge the combination of C_{pump} and C_{bad} , which here consists mostly of the parasitic capacitances of the diodes.

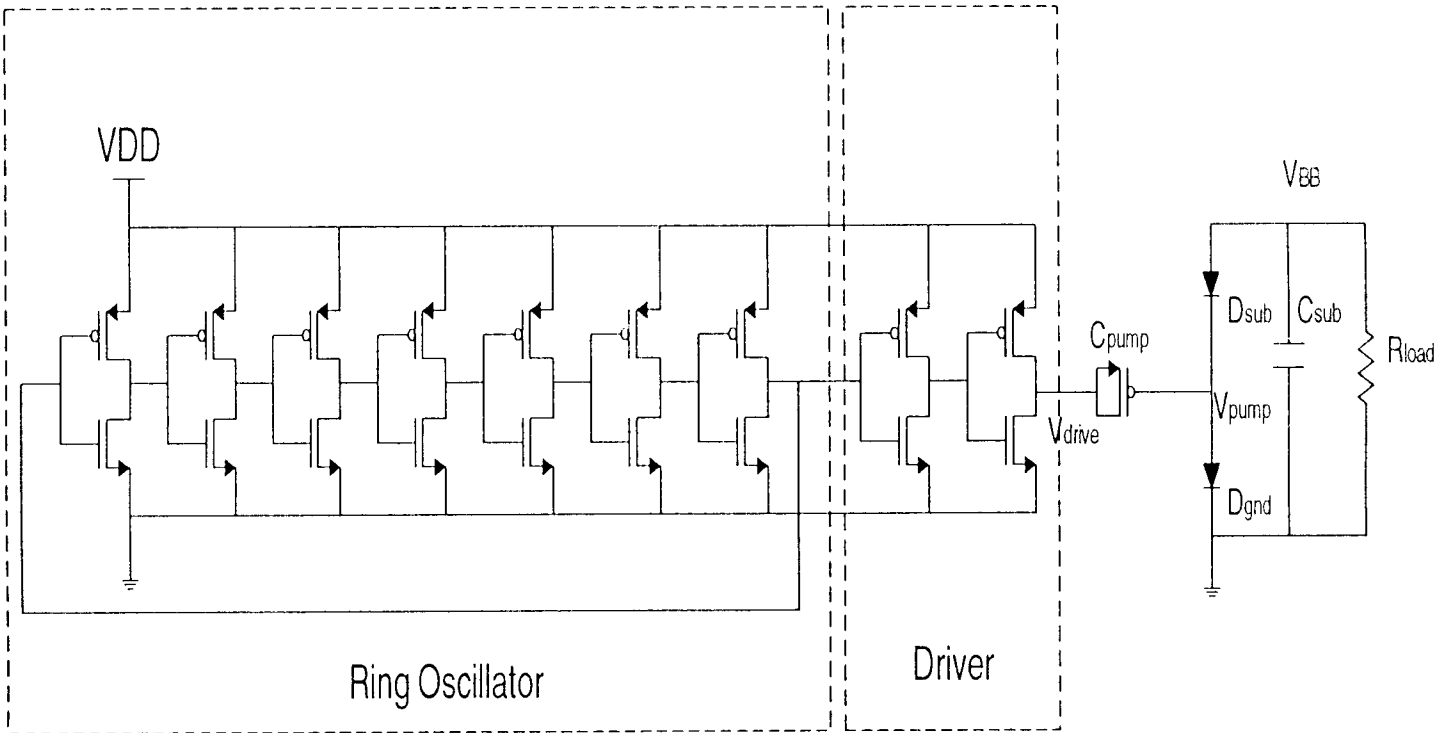


Figure 4. Schematic of Free-Run Pumping Circuit

Clearly, whenever the driver can charge the capacitors up in order to have a positive peak of V_{pump} greater than a diode drop within one half cycle of the ring oscillator frequency, the substrate voltage can be gradually brought down until it hits the value of $V_{\text{pump_negative-peak}}$ plus one diode drop.

Obviously, the output V_{BB} is not regulated over load and it would ideally approach $-V_{\text{DD}}$ plus two diode drops at steady state if the driver can keep up with the current need. Since our goal is to provide a relatively constant voltage within a range of load resistance (loading current greater than $10\mu\text{A}$), some kind of regulation should be provided.

A very straightforward approach to regulate the output voltage is to take advantage of the I-V characteristics of diodes when they are forward biased. Using the level 1 diode model, a forward current through the diode of around $10\mu\text{A}$ results in a voltage drop of about 0.45V. Three diodes in series would then provide roughly a 1.35V drop. Although this is inaccurate, it is more than adequate to meet the requirement for back biasing the substrates where the accuracy is not important.

The actual implementation of these diodes can be a P-active in n-well for each diode where the n-wells all have a higher potential than the substrate. A certain number of N-transistors configured as diodes while every transistor has a voltage drop of roughly V_t can be an alternative to the diode chain. The square law I-V relationship of MOS transistors provides a similar regulating scheme as the diodes. Figure 5 illustrates the diode I-V curve using level 1 diode model and the rest of the parameters shown in APPENDIX.

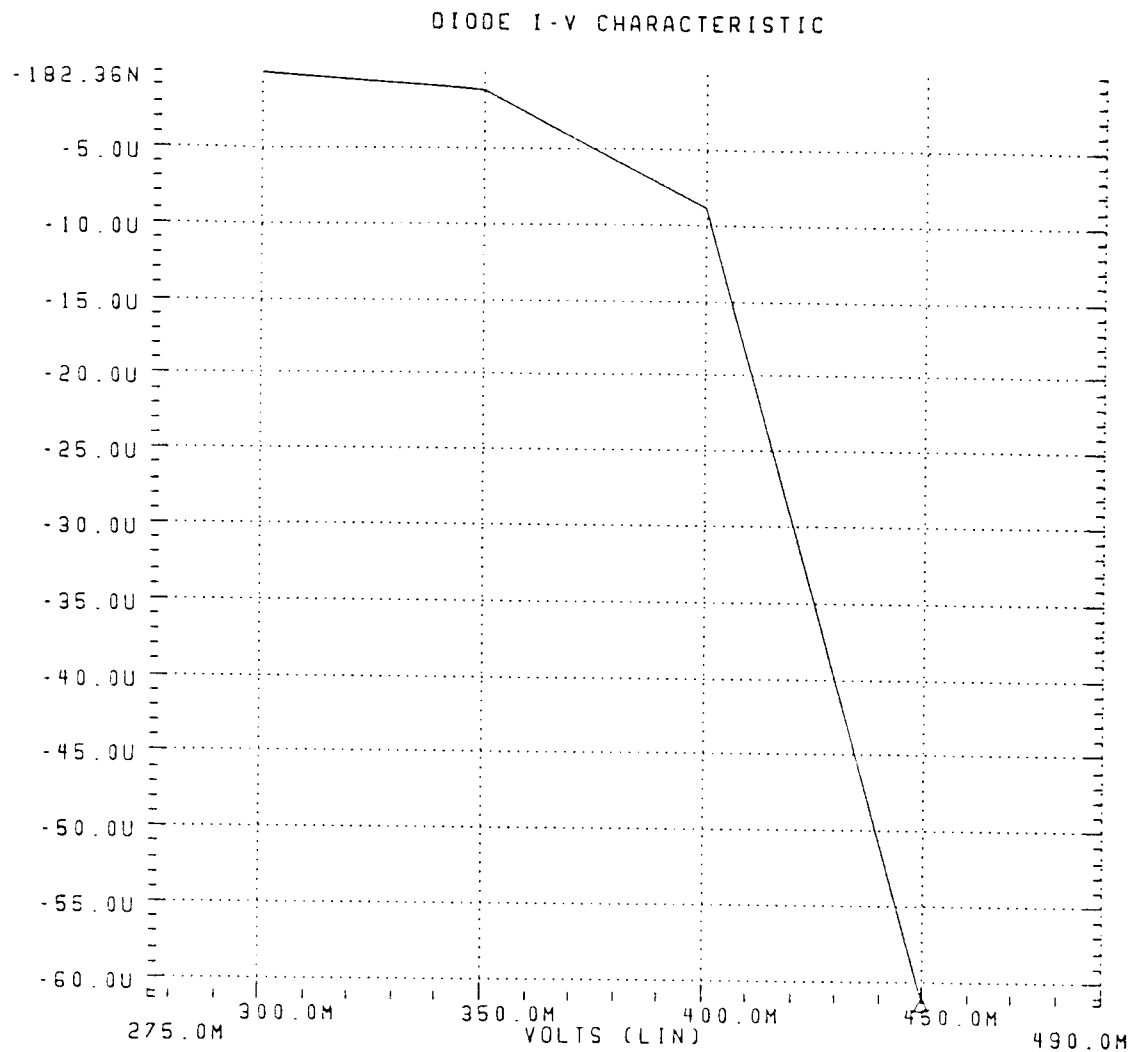


Figure 5. Diode I-V Curve.

Figure 6 is the complete circuit schematic with three regulating diodes in series. The ring oscillator consists of 7 identical size CMOS inverters; the driver shown following the ring oscillator includes two inverting amplifier in a row; the charge pump capacitor is made of a P-transistor with source and drain connected together. Also shown are the charge pump diodes, load capacitance, and load resistance.

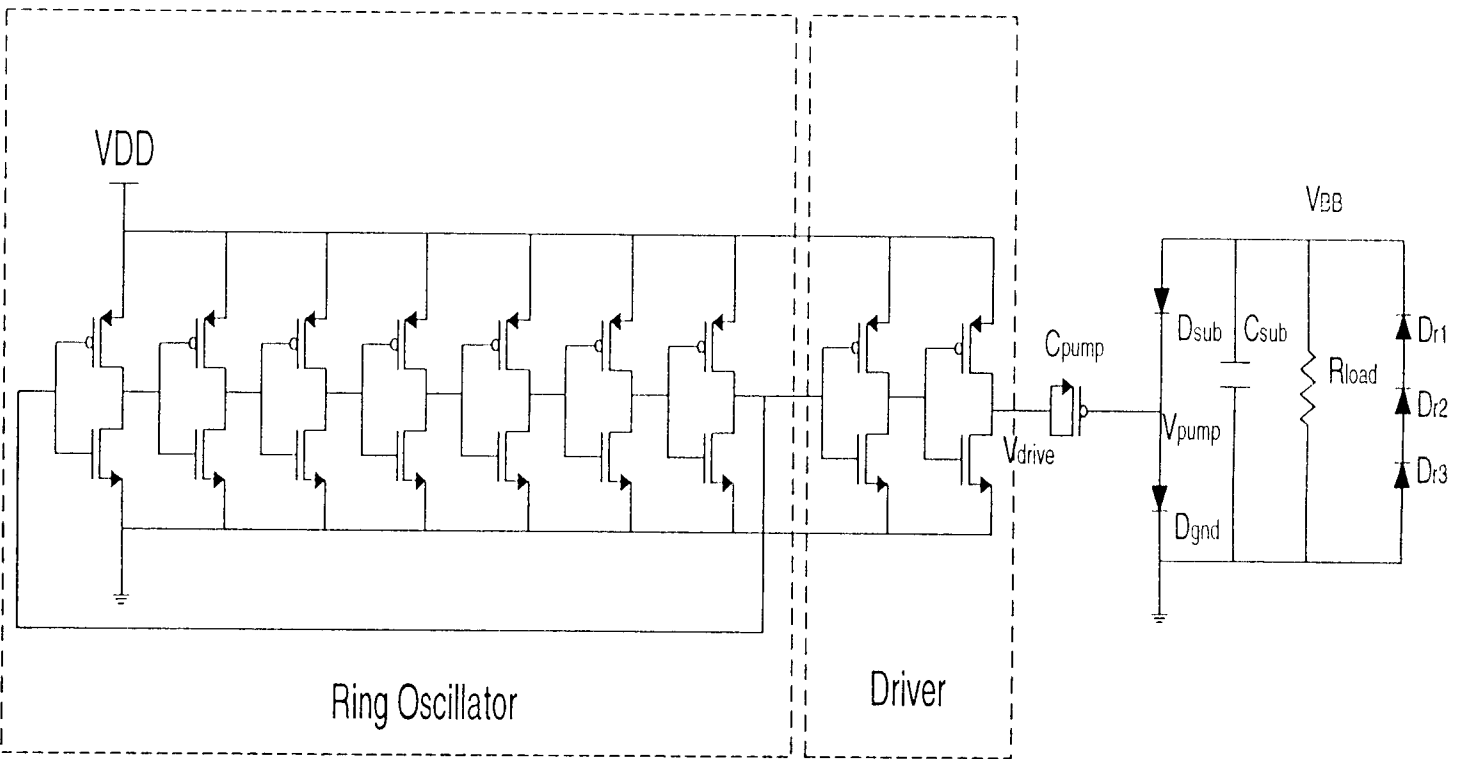


Figure 6. Schematic of Free-Run V_{BB} Generator With Regulating Diodes

The analysis and simulations are based on a P-substrate, 1.2um CMOS process, level 1 diode model and level 3 MOS model as included in the APPENDIX. HSPICE was used throughout the entire simulation.

A 7-stage ring oscillator is used to produce the 50MHz oscillation. To make the calculation process easier, every stage is chosen to be identical with respect to transistor sizes. The propagation delay for each stage is:

$$\tau_{delay} = \frac{1}{5 \times 10^7 \times 2N} = \frac{1}{5 \times 10^7 \times 2 \times 7} = 1.43ns \quad (5)$$

Each stage is a CMOS inverter. The P transistor size was chosen to be 3 times that of the n transistor for equal charging and discharging time, the n transistor sizing is about $w/l=1.8\mu m/4.2\mu m$ and p transistor as $5.4\mu m/4.2\mu m$. The driver following the ring oscillator is to charge the C_{pump} within at least one half of the oscillating cycle time as well as to sustain the steady state leakage current. Since the output stage of the ring oscillator is relatively weak in terms of current driving capability due to the transistor sizing, a two-stage inverter driver is used to magnify the current in order to have a at least $100\mu A$ peak driving current.

For the coupling capacitor, as discussed previously, a P-transistor with the source and drain connected is a suitable choice. When the body(n-well) is connected to V_{DD} , we don't have to worry about the forward biasing of p-substrate to n-well. With the source-drain connected to the charge pump, and the gate to the cathode of D_{sub} , the channel exists almost all the time since V_{pump} is always lower than or equal to V_{drive} . In other words, the transistor is in linear mode most of the time; thus C_{gd} and C_{gs} are relatively stable. If the transistor is ever turned off, the capacitance would drop by the factor of about a magnitude. Suppose the fringe capacitances are negligible, we

should have $C_{\text{equivalent}} \approx C_{\text{gd}} + C_{\text{gs}} = w l C_{\text{ox}}$, where for our CMOS process, $C_{\text{ox}} = 1.33\text{fF}/\mu\text{m}^2$. For $C_{\text{equivalent}} = 6\text{pF}$, assuming a square transistor, we have $w = l = 67\mu\text{m}$.

Extensive simulations were performed on both non-regulated circuits and circuits regulated with diodes. Since the dynamic performance of the circuits is difficult to calculate, various combinations of oscillating frequency, charge pump capacitors, and load resistances are simulated. Figure 7 shows the results of C_{pump} dimension (square transistor, $w = l$) vs. V_{BB} voltage output when oscillating frequency $f = 50\text{MHz}$, load resistance $R_{\text{load}} = 500\text{k}\Omega$, the second stage driver size of $(w/l)_n = 8.4\mu\text{m}/1.2\mu\text{m}$ and $(w/l)_p = 24\mu\text{m}/1.2\mu\text{m}$.

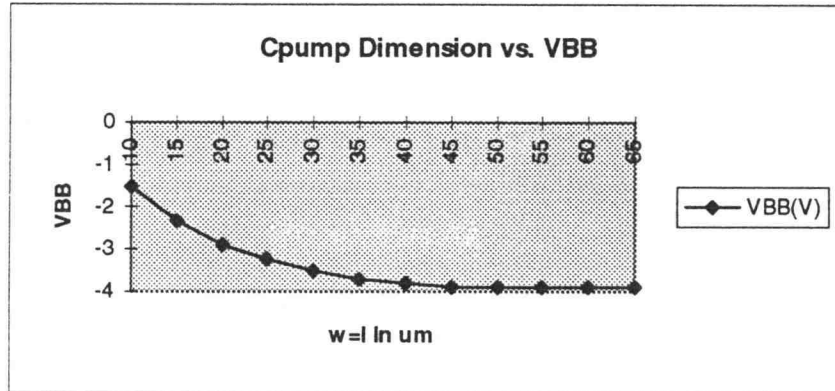


Figure 7. C_{pump} Dimension vs. V_{BB} of Free-Run Circuit

Clearly, the absolute value of output voltage increases with the increase of the dimension of the charge pump capacitor. When the dimension reaches $w = l = 45\mu\text{m}$, the output voltage reaches its peak value and stays at -3.9V as the dimension (the charge pump capacitance) further increases.

A reasonable substrate capacitance is within $100\text{pF} \sim 1000\text{pF}$ range. This capacitance serves as a low pass filter to smooth the V_{BB} output. Figure 8 is a

simulated transient output of V_{BB} with $C_{sub} = 10\text{pF}$ and C_{pump} size of $w = l = 60\mu\text{m}$. To speed up the simulation, a C_{sub} of 10pF was used. The ripple is about 50mV peak to peak and can be further reduced if the C_{sub} is chosen larger, which is the reality in most cases. A load resistance of $500\text{ k}\Omega$ is used as a typical value.

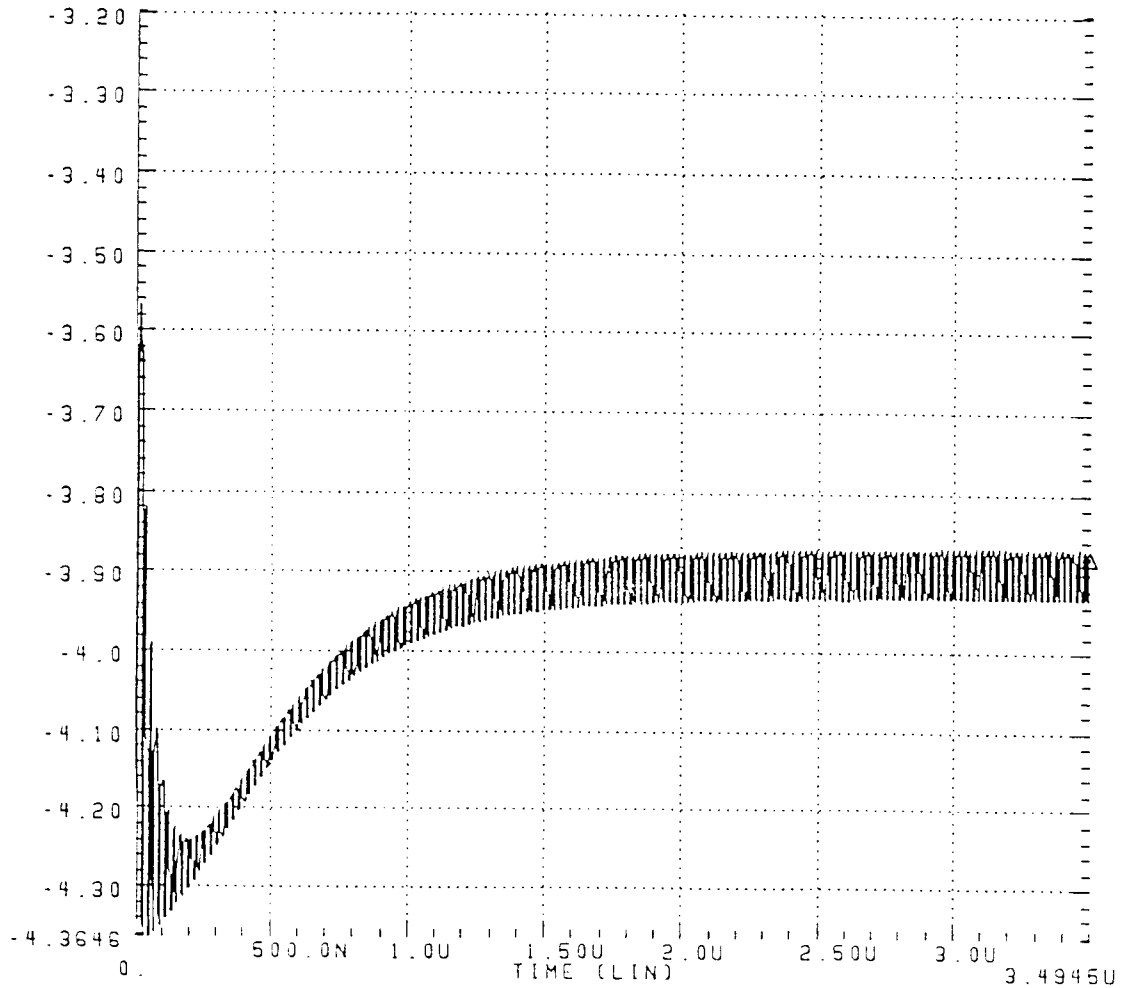


Figure 8. Transient V_{BB} Output of Free-Run Circuit

Figure 9 shows the results of oscillating frequency f vs. V_{BB} voltage output when C_{pump} size is $w = l = 60\mu\text{m}$, and load resistance = $500\text{ k}\Omega$.

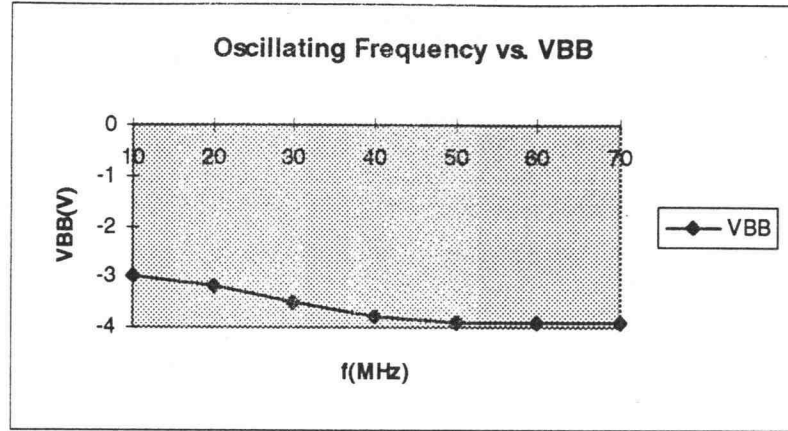


Figure 9. Oscillating Frequency vs. V_{BB} of Free-Run Circuit

The output magnitude is dependent upon the oscillating frequency. The higher the frequency, the higher the absolute output voltage until the pumping rate can keep up with the current loss. Since the ripple frequency is obviously related to the charge pump frequency, the higher the oscillating frequency, the smaller the C_{sub} required to achieve the same ripple percentage. This is a compromise with the size of C_{pump} transistor. The reason we want the f to be relatively high is mainly because of the need to keep the C_{pump} size small.

Figure 10 shows the simulation results of load resistance vs. V_{BB} voltage output when oscillating frequency $f = 50\text{MHz}$, C_{pump} size is $w = l = 60\mu\text{m}$.

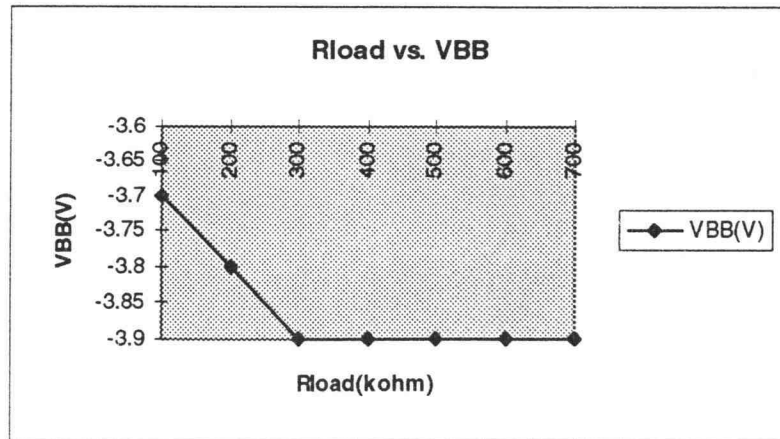


Figure 10. R_{load} vs. V_{BB} of Free-Run Circuit

The above simulations demonstrate the relationship among C_{pump} , R_{load} , and pumping frequency using the free-run non-regulated circuit. Practically, our primary concern is the load regulation since this is the only parameter that changes from chip to chip.

Figure 11 shows the simulation results of load resistance vs. V_{BB} voltage output when C_{pump} size is $w = l = 40\mu\text{m}$, oscillating frequency $f = 50\text{MHz}$, and with three regulating diodes in series.

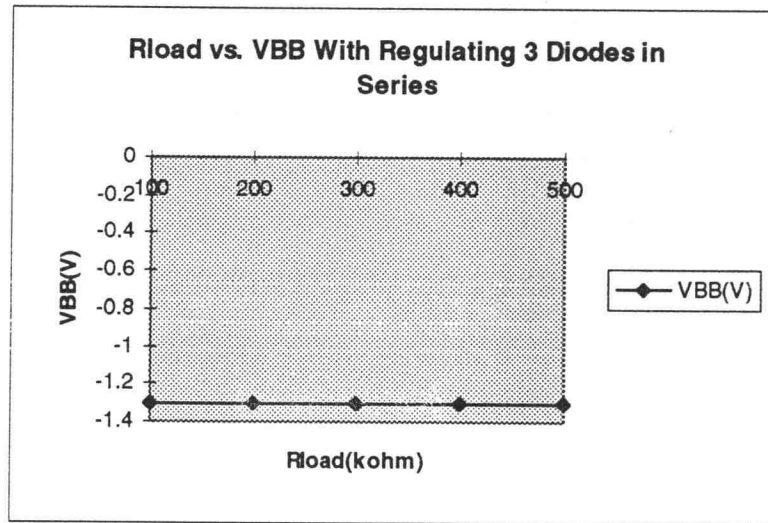


Figure 11. R_{load} vs. V_{BB} of Free-Run Circuit with 3 Regulating Diodes in Series

This chart proves that with diodes in parallel with the load, a very good load regulation can be achieved. Figure 12 is a simulated transient output of V_{BB} with $C_{\text{sub}} = 100\text{pF}$, $f = 50\text{MHz}$, $R_{\text{load}} = 500\text{k}\Omega$, and C_{pump} size of $w = l = 40\mu\text{m}$. Notice that the output voltage is regulated at about -1.33V . The ripple peak-to-peak voltage is about 40mV when 100pF C_{sub} is used.

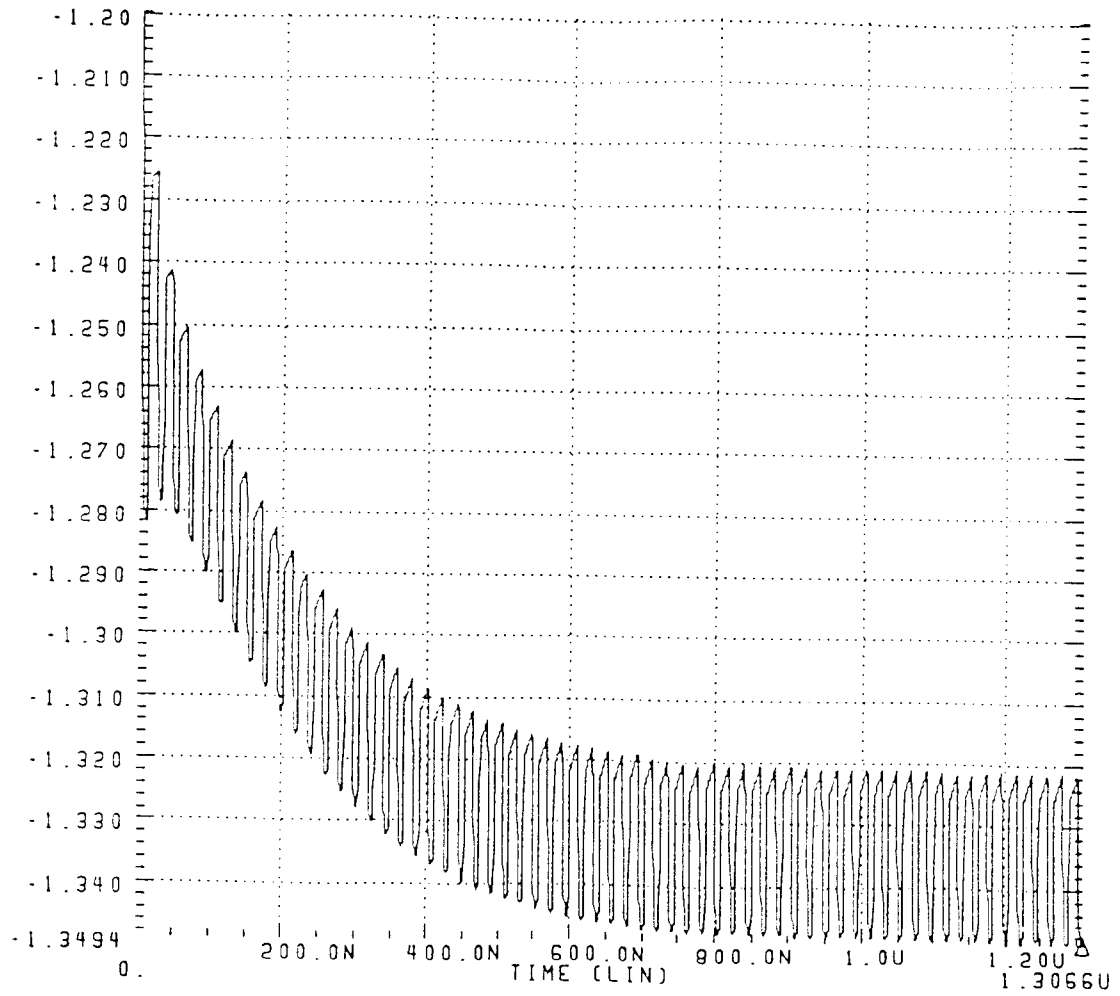


Figure 12. Transient V_{BB} Output with 3 Regulating Diodes

Figure 13 shows results of oscillating frequency f vs. V_{BB} voltage output when C_{pump} size is $w = l = 60\mu\text{m}$, load resistance = $500\text{k}\Omega$, and with 3 regulating diodes in series.

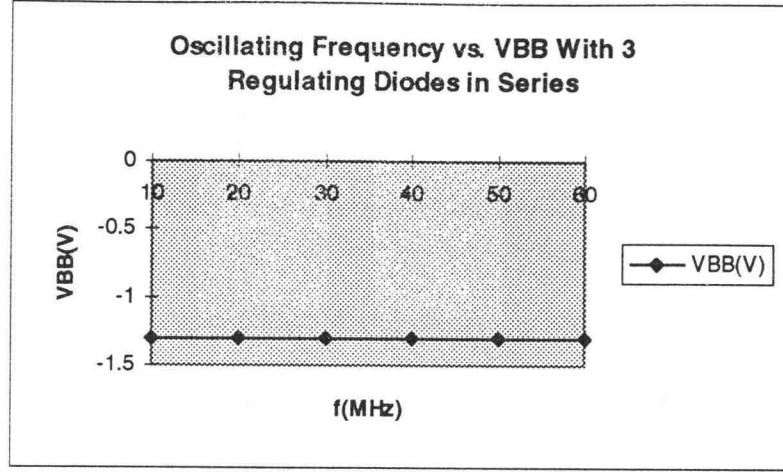


Figure 13. Oscillating Frequency vs. V_{BB} with 3 Regulating Diodes

4.1.2 Current Source Generator for Guard Ring Diodes

The anodes of guard ring diodes are P-substrate. The heavily doped n regions are the cathodes of the diodes. We have generated -1.3V substrate bias which is regulated by 3 forward biased diodes in series, and the regulated output voltage is basically load independent over the load range of $100k\Omega$ to $1M\Omega$. This substrate bias is applied at the anode of the guard ring diode. In order to forward bias the guard ring diode, its cathode needs to be at an even lower potential. Our interest is to generate a controllable current through the guard ring diode with a range of $2\mu A$ to $20\mu A$. Since the I-V characteristics of diode is exponential, it is difficult to determine the current by directly applying voltages across the diode.

A current sink or source can be used to generate a constant current [10]. Based on two facts: first, the forward biased diode has a voltage drop of roughly 0.4V across it when the forward current is around $5\mu A$ and basically does not change much (Figure 5) over the current range of $2\mu A$ to $20\mu A$; second, by setting MOS transistors in saturation mode, the drain-source current can be solely controlled by gate-source

voltage. Taking advantage of these two facts and having been able to regulate the substrate bias, a current source can be generated as shown in Figure 14.

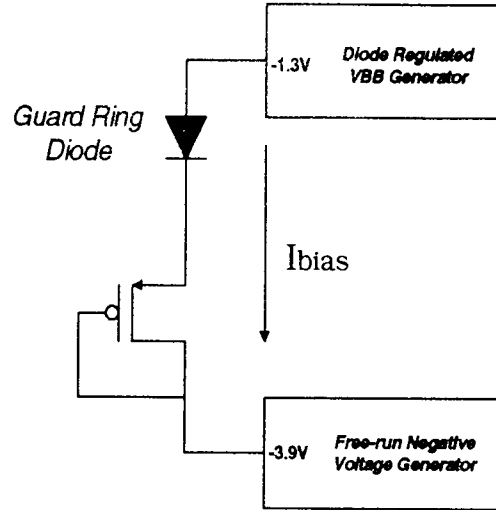


Figure 14. Current Source Generator with Free-Run Circuits

The reason for using a P transistor as a current source instead of N-transistor as a current sink is because of the concern of the CMOS process. Since generally n-wells are connected to V_{DD} (or as high as possible), and both P substrate and source-drain of this transistor are below ground, there is no risk of forward biasing the P-N junctions, although the sizing of P-transistor is a disadvantage over N-transistor for achieving same amount of current.

The following equation illustrates the relationship between the threshold voltage of the transistor and V_{SB} :

$$V_{tp} = V_{tp0} + \gamma (\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}) \quad (6)$$

Clearly we want to minimize the V_{SB} in order to minimize the threshold voltage and furthermore minimize the transistor size to generate same amount of current. To do so the n-well body can be grounded for this transistor instead of connected to the V_{DD} . In this circuit two negative voltages need to be generated. One is for back biasing the substrate while another one, V_{neg} , is for forward biasing the guard ring diode. Actually both generators can share the same ring oscillator and driver with some adjustments for the driver's size to pump two circuits. The diode regulated V_{BB} generator is used for the substrate bias which is at about -1.3V; the voltage V_{neg} is generated with a free run negative voltage generator without regulating diodes which produces a minimum voltage of -3.9V. By adjusting the size of the current source P transistor, a controllable current source can be generated.

An issue arises when generating the V_{neg} where we can no longer take advantage of the substrate capacitance. To keep the ripple low enough, an off-chip capacitor is needed and great care needs to be taken to minimize the bonding wire inductance.

Figure 15 is the schematic of current source generator using two free-run negative voltage generator circuits. Note only one ring oscillator and driver are used for both pumping circuits.

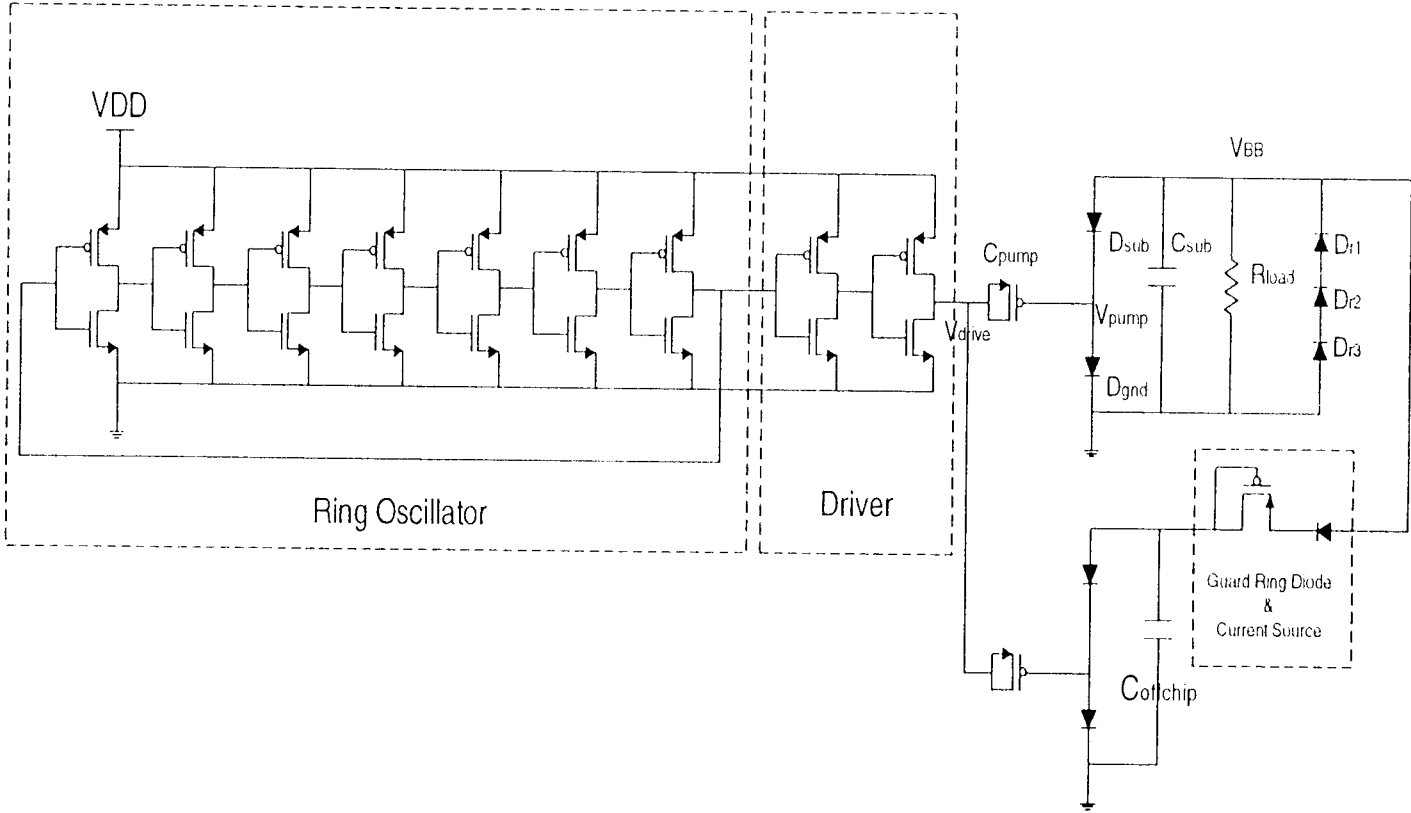


Figure 15. Schematic of Current Source Generator with Free-Run Circuits

Following we will calculate the P-transistor sizes:

Since we are biasing the substrate at about -1.3V, i.e. $V_{BB} = -1.3V$, according to equation (6), and

$$V_{SB} \approx -1.3V - 0.4V = -1.7V.$$

From level 3 MOS model, $\phi_F = 0.6V$, $V_{tp0} = -0.8406V$ and $\gamma = -0.5768$.

We have

$$V_{tp} = -0.8406 - 0.5768(\sqrt{-2 \times 0.6 - 1.7} - \sqrt{-2 \times 0.6}) = -1.1904V \quad (7)$$

The P transistor is configured as a diode by connecting the gate and the drain. If $V_{gs} < V_{tp}$, the transistor will always be in saturation mode. Thus we have

$$I_D = \frac{1}{2} k_p \left(\frac{w}{l}\right)_p (V_{sg} - |V_{tp}|)^2 \quad (8)$$

We have demonstrated that a regulated V_{BB} at -1.3V and a non-regulated V_{neg} of about -3.9V can be generated. The -3.9V is relatively load independent when the load resistance is greater than 200k Ω . Refer to Figure 4, a total voltage across the guard ring diode and the P transistor is about 2.6V. Voltages at both ends are load independent if the current through the guard ring diode is small.

If the voltage drop on the diode is about 0.4V, then $V_{sg} \approx 2.6 - 0.4 = 2.2V$. From equation (8), with $k_p = 2.545E-5 \text{ A/V}^2$, $V_{tp} = -1.1904V$, we can generate the following table:

$I_{bias}(\mu A)$	Possible Transistor Sizes(μm)	
	w	l
2	1.8	12
4	1.8	6
6	5.4	12
8	1.8	3
10	1.8	2.4
12	5.4	6
14	12.6	12
16	3.6	3
18	16.2	12
20	1.8	1.2

Table 1. Calculated Current vs. Transistor Sizes with Free-Run Circuits

Simulations were performed for each of the above calculations assuming a 100pF off-chip capacitor is connected to node V_{neg} . Also the substrate capacitance is assumed as 100pF. Actually the two capacitor values can be a magnitude higher. The reason for choosing 100pF is due to the simulating time constraint.

Figure 16 is a simulated current generated using this circuit. The circuit parameters are set to generate a 4uA current source. As can be seen, the output at steady state is about 2uA. In Figure 16 also shown are V_{BB} and V_{neg} which are at steady state about 0.1V off from the value used for calculating the current. Apparently the inaccuracy of these voltages is the major reason that the current output is far from

what we expected. Table 2 gives the comparison between calculated and simulated current.

As can be seen, the percentage errors are quite large. This is mainly because the actual voltages generated from both free-run negative voltage generator are not precisely what we expected. Also since the two voltage outputs vary as loads change, we can expect that the current generated this way can be really off the mark. To predict an accurate current output is very difficult.

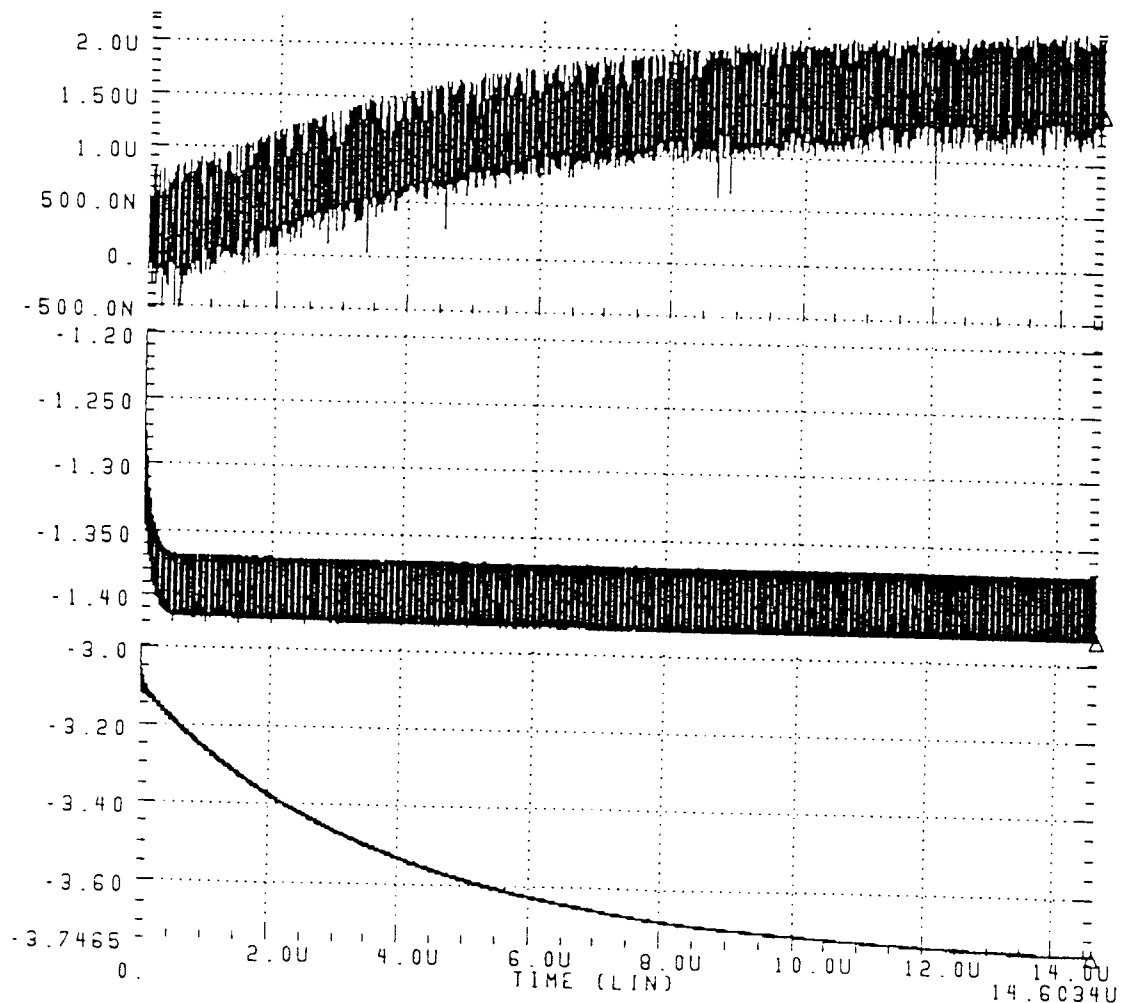


Figure 16. Transient Current Output with Free-Run Circuits.

Transistor Sizes(μm)		Current(μA)		error(%)
w	l	Calculated	Simulated	
1.8	12	2	1.1	45
1.8	6	4	1.9	52.5
5.4	12	6	3.2	46.6
1.8	3	8	3.9	51.25
1.8	2.4	10	4.8	52
5.4	6	12	6.3	47.5
12.6	12	14	7	50
3.6	3	16	8.5	46.87
16.2	12	18	9.5	47.22
1.8	1.2	20	11	45

Table 2. Comparison of Calculated and Simulated Current Generated with Free-Run Circuits.

4.2 Circuits with Feedback Loop Regulation

The circuits in the last section have apparent drawbacks. Since this is basically a free-run circuit, precise voltage control can not be really achieved. This seems to be fine when only substrate bias is needed, since the accuracy of back bias is not of great significance. But when an accurate current source needs to be generated accurate voltage sources must be generated first, and this needs good load regulation and precise output voltage control.

Due to the considerations above, feedback needs to be introduced in generating the negative voltages in order to regulate the outputs, mostly for the load regulation. Circuits with feedback loop regulation are introduced below, taking advantages of MOS transistor characteristics.

4.2.1 Negative Voltage Generator

Figure 17 is the basic block diagram of the circuit to generate regulated negative substrate bias.

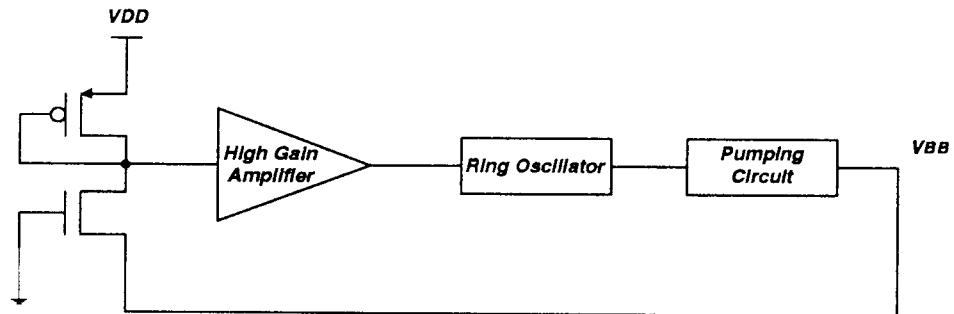


Figure 17. Block Diagram of Feedback Loop Regulated V_{BB} Generator

There are three parts in this circuit: an oscillator control section that maintains a pre-determined V_{BB} by inhibiting and enabling the oscillator to limit the pumping action, a ring oscillator with output stage driver, and a pumping network capable of driving the output node to negative.

The P-transistor's gate is connected to the drain, so that the transistor is always operated in saturation mode if $V_{sg} > |V_{tp}|$. The n-transistor's gate is grounded and the source is connected to the substrate.

Following the P and N transistors is a high gain stage with a voltage gain of at least 60db which is made of 4 CMOS inverters. The output voltage of the high gain amplifier is high when the input node is higher than the switch point V_{sw} of the first inverter and is low when the input node is lower than switch point. This stage amplifies

a small voltage change at the input node to full voltage swing and powers the following ring oscillator. The power for the ring oscillator is provided by the output of the high gain amplifier. When the output of the high gain amplifier is high, the ring oscillator oscillates and stops oscillating when the output of the amplifier is low.

The pumping network is basically the same as described before. When the voltage at the input of the high gain amplifier is below the switch point of the first stage inverter, the charge pump stops pumping the substrate to more negative. When the voltage at the input of the high gain amplifier is higher than switch point, the pump will start and pump the substrate to more negative. This action keeps voltage at the input of the high gain amplifier at the switch voltage point of the first inverter and thus keeps the V_{BB} at a certain negative voltage level.

Figure 18 is the complete schematic of feedback loop regulated substrate bias generator. Through the operation both M1 and M2 are in saturation mode, so we have the following equation:

$$\frac{1}{2}k_p\left(\frac{w}{l}\right)_p(V_{sgp}-|V_{tp}|)^2 = \frac{1}{2}k_n\left(\frac{w}{l}\right)_n(V_{gsn}-V_{tn})^2 \quad (9)$$

and

$$V_{gsn} = 0 - V_{BB}, \quad V_{sgp} = V_{DD} - V_{sw}$$

Substitute them into equation (9), we have

$$\frac{1}{2}k_p\left(\frac{w}{l}\right)_p(V_{DD}-V_{sw}-|V_{tp}|)^2 = \frac{1}{2}k_n\left(\frac{w}{l}\right)_n(-V_{BB}-V_{tn})^2 \quad (10)$$

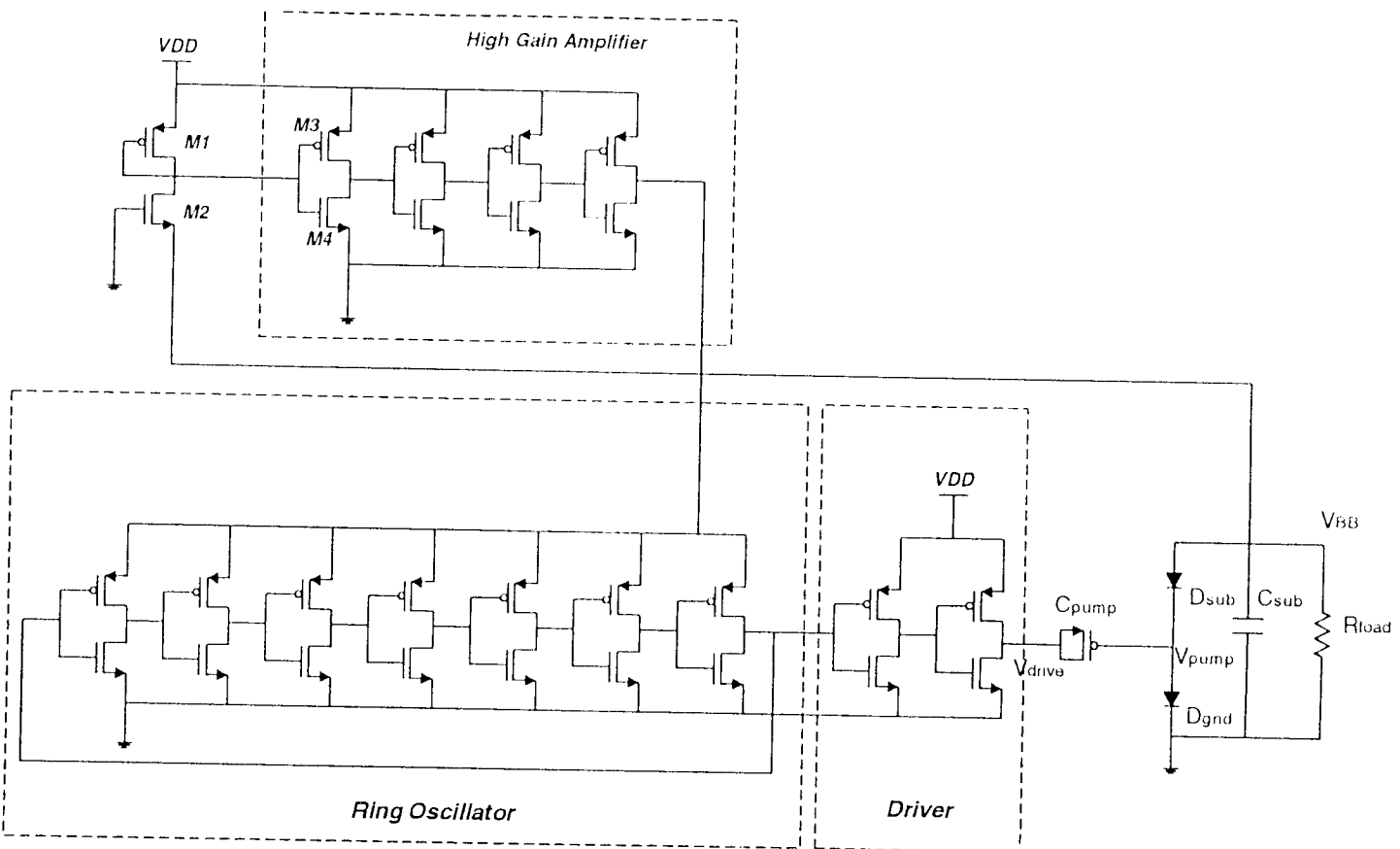


Figure 18. Schematic of Feedback Loop Regulated V_{BB} Generator

then

$$-V_{BB} = \sqrt{\frac{k_p (\frac{w}{l})_p}{k_n (\frac{w}{l})_n}} (V_{DD} - V_{sw} - |V_{tp}|) + V_{in} \quad (11)$$

Now we will calculate the V_{sw} of the input stage inverter of the high gain amplifier. The device sizes of this inverter are chosen as:

p-transistor: $(w/l)_p = 5.4\mu\text{m}/1.2\mu\text{m}$

n-transistor: $(w/l)_n = 1.8\mu\text{m}/1.2\mu\text{m}$

That is

$$\frac{(w/l)_p}{(w/l)_n} = 3 \quad (12)$$

In level 3 MOS model,

$$k_p = 2.5454\text{E-}5 \text{ A/V}^2$$

$$k_n = 8.3843\text{E-}5 \text{ A/V}^2$$

$$V_{sw} = \frac{V_{DD} - |V_{tp}| + V_{in} \sqrt{\frac{k_n(w/l)_n}{k_p(w/l)_p}}}{1 + \sqrt{\frac{k_n(w/l)_n}{k_p(w/l)_p}}} \quad (13)$$

Here,

$$V_{DD} = +5V, \quad V_{tp} = 0.84V.$$

Since p substrate is biased at V_{BB} , V_{in} is calculated as

$$V_{in} = V_{in0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}) \quad (14)$$

with $V_{SB} = 0 - V_{BB}$, we then have

$$V_{in} = V_{in0} + \gamma(\sqrt{|-2\phi_F - V_{BB}|} - \sqrt{|-2\phi_F|}) \quad (15)$$

here

$$\gamma = 0.7792, \quad \phi_F = -0.6V \text{ and } V_{in0} = 0.9573V$$

Then

$$\begin{aligned} V_{in} &= 0.9573 + 0.7792(\sqrt{|2 \times 0.6 - V_{BB}|} - \sqrt{|2 \times 0.6|}) \\ &= 0.1038 + 0.7792\sqrt{|1.2 - V_{BB}|} \end{aligned} \quad (16)$$

Substitute (16) into equation (13)

$$V_{sw} = 2.0846 + 0.3987\sqrt{1.2 - V_{BB}} \quad (17)$$

Substituting (17) into (11) we can derive a relationship between V_{BB} and the transistor size ratio. By choosing the appropriate ratio of M1 and M2 sizes, the desired V_{BB} can be precisely generated. In practice the transistors M1 and M2 can be made very low gain, thus have very small current during the operation. Combining equation (11) and (17), a table can be generated for choosing M1 and M2 sizes to produce desirable substrate biases. (tolerance of transistor sizes are within 2% of calculated value)

$V_{BB}(V)$	$V_{sw}(V)$	Possible sizes			
		$(w/l)_p/(w/l)_n$	$w_n(\mu m)$	$w_p(\mu m)$	$l_p=l_n(\mu m)$
-1	2.68	0.0027	666	1.8	24
-1.5	2.74	0.4795	12.6	6	24
-2	2.80	1.9308	1.8	3.6	24
-2.5	2.86	4.6266	1.8	8.4	24
-3	2.90	8.6356	1.8	15.6	24
-3.5	2.95	14.51	2.4	34.82	24

Table 3. Calculated Transistor Sizes of Feedback Loop Regulated V_{BB} Generator

The high gain amplifier should be able to supply the current that the ring oscillator needs during oscillation operation while the output stage of the amplifier is high. This requires the P-transistor of the last amplifier stage be large enough to

sustain the supply current for the ring oscillator. Also the gain of at least 60dB indicates that when the input has a 5mV change the output should rail. This promises that the input voltage is always kept at $V_{sw} \pm 5\text{mV}$.

Figure 19 illustrates a simulated voltage output of this circuit when the M1 and M2 sizes are set to generate a V_{BB} of -1.5V. The first output is the V_{BB} and its voltage is about -1.5V. The second part of the graph shows the behavior of the ring oscillator power which initially is high to keep pumping the circuit until the V_{BB} reaches about -1.5V. It clearly demonstrates the ‘on-off’ actions. The third part of the graph is the output of the ring oscillator. It corresponds to the ring oscillator power to be ‘on’ or ‘off’.

This circuit gives excellent load regulation. While R_{load} changes from 100k Ω to 1M Ω , the output voltage virtually does not change at all.

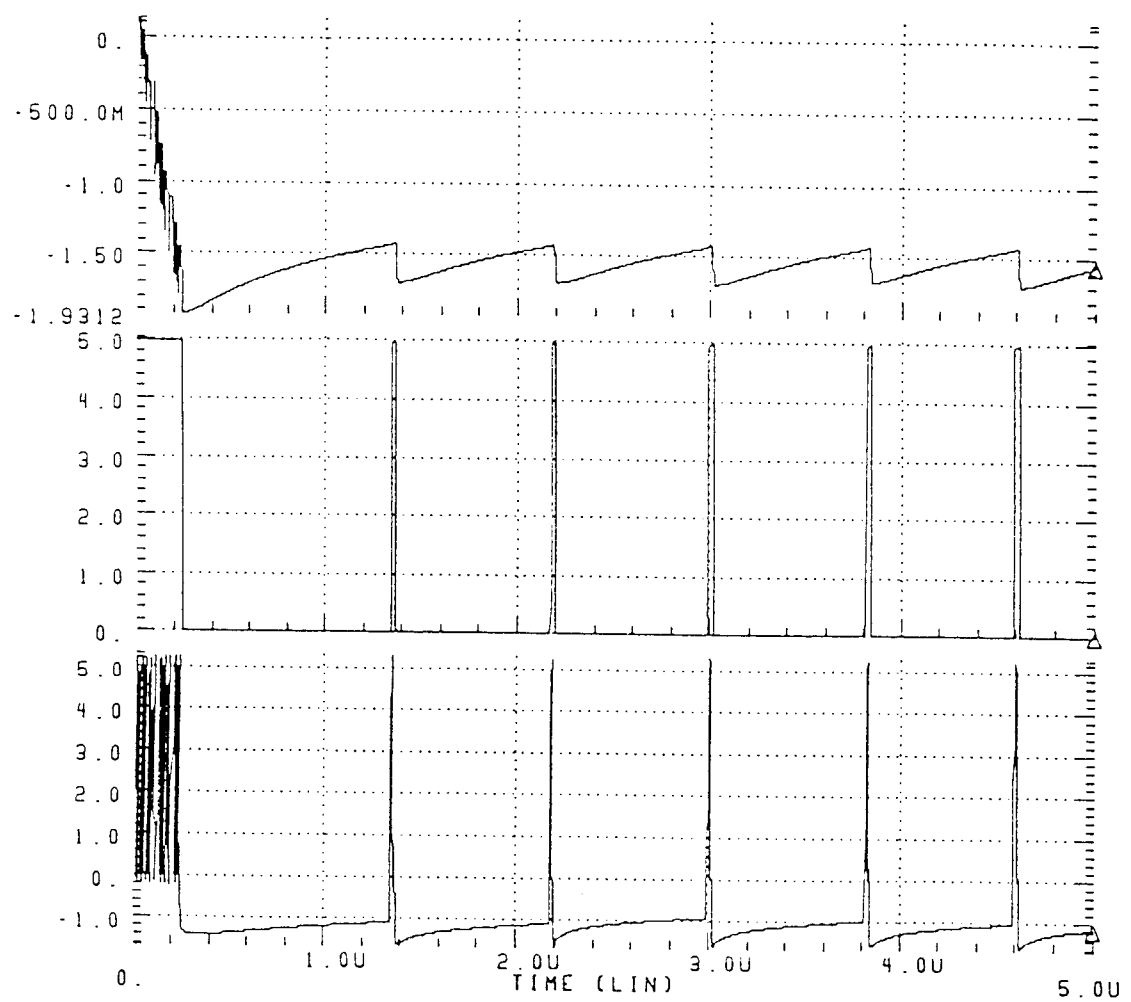


Figure 19. A Simulated Voltage Output of Feedback Regulated V_{BB} Generator

M1 and M2 sizes						
$(w/l)_p/(w/l)_n$	$w_n(\mu m)$	$w_p(\mu m)$	$l_p=l_n(\mu m)$	Calculated(V)	Simulated(V)	Error(%)
0.0027	666	1.8	24	-1	-1.05	5
0.4795	12.6	6	24	-1.5	-1.55	3
1.9308	1.8	3.6	24	-2	-2.1	5
4.6266	1.8	8.4	24	-2.5	-2.6	4
8.6356	1.8	15.6	24	-3	-3.1	3
14.51	2.4	34.82	24	-3.5	-3.5	0

Table 4. Comparison of Calculated and Simulated Results of Feedback Loop Regulated V_{BB} Generator

Table 4 illustrates the comparison between calculated and simulated voltages. As we can see, the output voltages simulated are very close to the values calculated. The major error source is the round off of transistor sizes during calculation. Along with the excellent load regulation, this provides us a good regulated voltage for generating the current source.

4.2.2 Current Source Generator

Again with the regulated approach the controllable current source can be generated exploiting the I-V characteristics of MOS transistor. In the last discussion we were able to generate well-controllable and regulated substrate bias. The current source can still be generated with the same configuration, but now we have much improved voltage references shown in Figure 20.

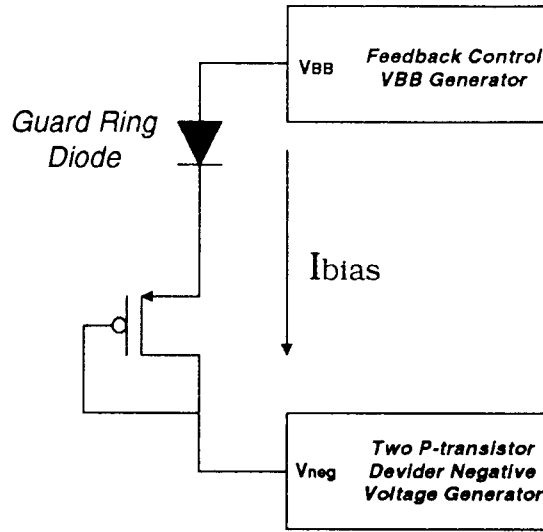


Figure 20. Current Source Generator with Feedback Loop Regulated Circuits

V_{BB} can be generated with the circuit introduced in the last discussion, i.e. the voltage divider at the first stage is a CMOS pair. But the more negative voltage V_{neg} here cannot be produced using exactly the same method since the source voltage level of M2 would be lower than that of the M2 body, assuming the body is connected to V_{BB} . Therefore some modification must be considered. To solve this problem we can replace M2 with a P-transistor whose drain and gate are connected together to V_{neg} . This actually forms a voltage divider with P-transistors M1 and M2.

Figure 21 is the schematic of this two P-transistor divider circuit. The rest of the circuit is exactly the same as the previous circuit. We will calculate the device sizes for this Two P-transistor divider circuit. Choose to bias the substrate at -1.5V using the CMOS-divider regulated V_{BB} generator. From table 3, the switch point of the input inverter of high gain amplifier is 2.74V. Since current flowing through M1 and M2 are always identical, we have,

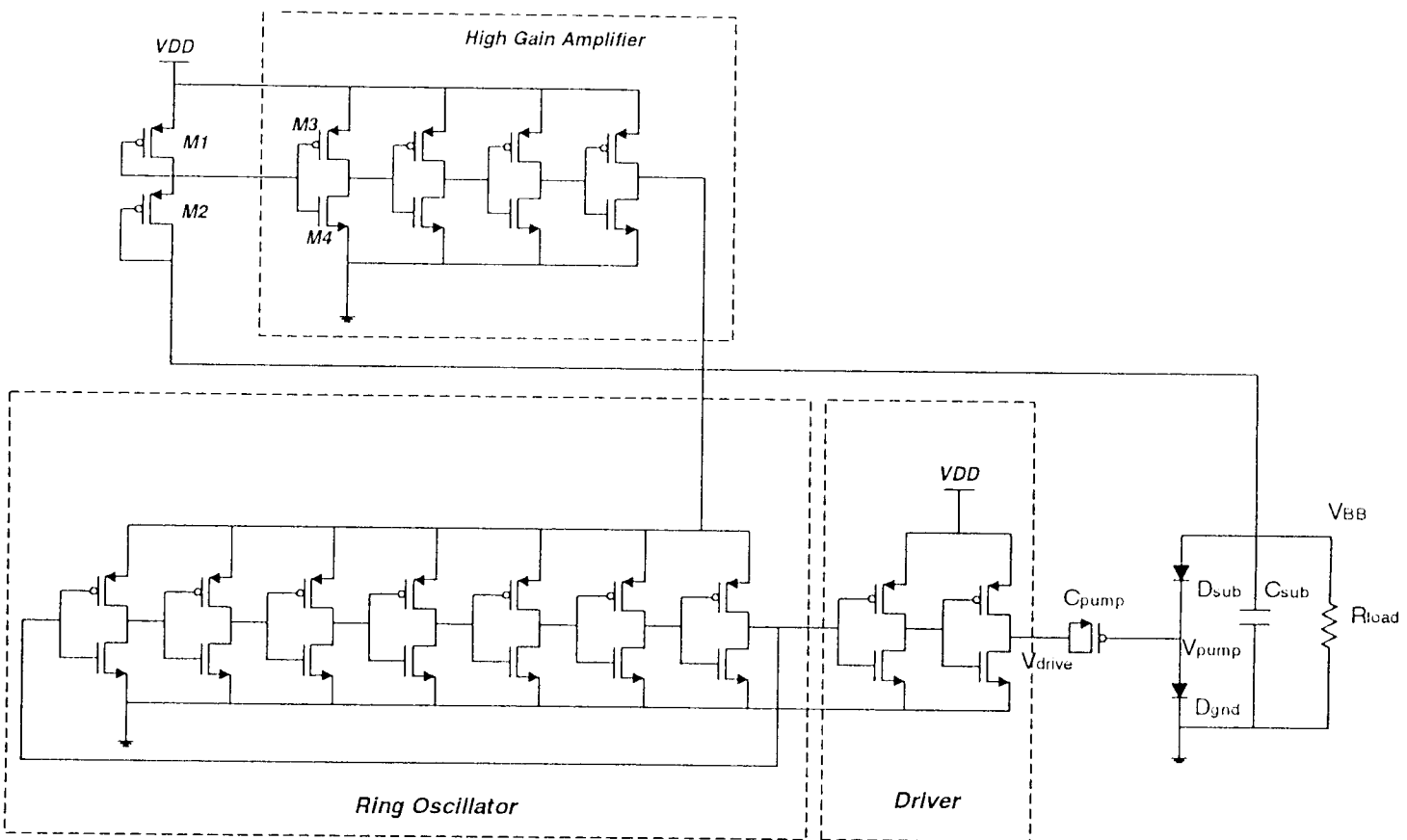


Figure 21. Schematic of Two PMOS Divider Circuit

$$\frac{1}{2}k_p(w/l)_{M1}(V_{DD} - V_{sw} - |V_{tpM1}|)^2 = \frac{1}{2}k_p(w/l)_{M2}(V_{sw} - V_{neg} - |V_{tpM2}|)^2 \quad (18)$$

here because $V_{SBM1} = 0$,

$$V_{tpM1} = V_{tp0} = 0.8406V \quad (19)$$

at steady state, $V_{SBM2} = V_{sw} - V_{DD} = 2.74 - 5 = -2.26V$,

$$\begin{aligned} V_{tpM2} &= V_{tp0} + \gamma(\sqrt{|-2\phi_F + V_{SBM2}|} - \sqrt{|-2\phi_F|}) \\ &= -0.8406 - 0.5768(\sqrt{|-2 \times 0.6 - 2.26|} - \sqrt{|-2 \times 0.6|}) = -1.2817V \end{aligned} \quad (20)$$

From equation (18)

$$-V_{neg} = \sqrt{\frac{(w/l)_{M1}}{(w/l)_{M2}}}(V_{DD} - V_{sw} - |V_{tpM1}|) + |V_{tpM2}| - V_{sw} \quad (21)$$

In this case,

$$V_{DD} = 5V, \quad V_{sw} = 2.74V, \quad V_{tpM1} = 0.8406V \text{ and } V_{tpM2} = -1.2817V$$

Then

$$V_{neg} = -1.42 \sqrt{\frac{(w/l)_{M1}}{(w/l)_{M2}}} + 1.46 \quad (22)$$

A table again can be generated according to the above equation:

		Possible sizes		
Vneg(V)	(w/l) _{M1} /(w/l) _{M2}	w _{M1} (um)	w _{M2} (um)	l _{M1} =l _{M2} (um)
-1	3.00	6	1.8	24
-1.5	4.35	7.8	1.8	24
-2	5.94	10.8	1.8	24
-2.5	7.78	18.6	2.4	24
-3	9.86	18	1.8	24
-3.5	12.20	25.2	1.8	24

Table 5. Calculated Transistor Sizes of Two P Transistor Divider Circuit

Figure 22 is the simulated transient result for this two P-transistor divider circuit while the M1 and M2 sizes are set to generate a V_{neg} of -3.5V according to table 5. The first part of the graph illustrates the V_{neg} . As can be observed, it is very close to the calculated value. The second and third part of the graph are the ring oscillator power and output. Like the first feedback loop regulated circuit, the ring oscillator and its power behave similarly to turn the oscillator 'on' or 'off' while the V_{neg} is bouncing around -3.5V.

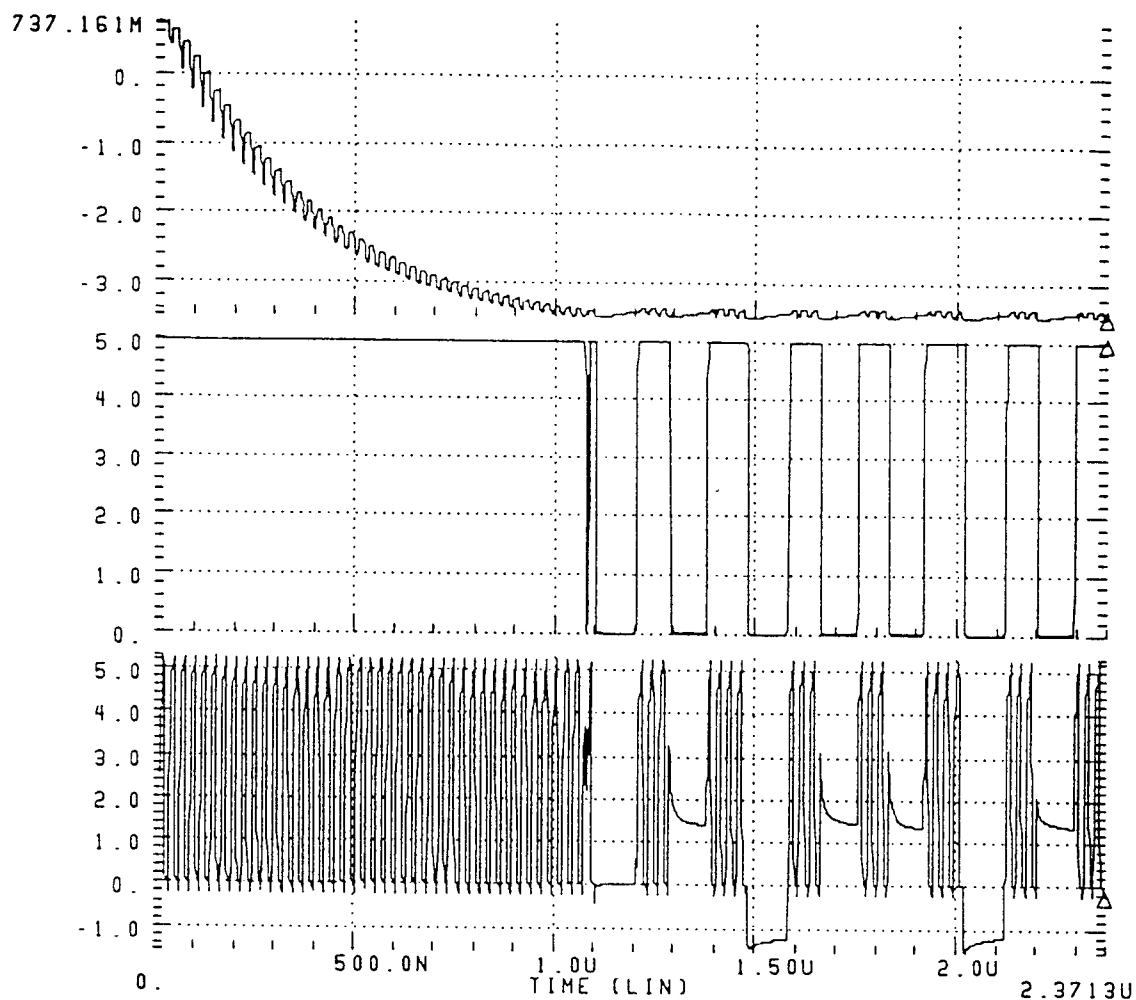


Figure 22. A simulated Voltage Output of Two P Transistor Divider Circuit

M1 and M2 sizes						
$(w/l)_{M1}/(w/l)_{M2}$	$w_{M1}(\mu m)$	$w_{M2}(\mu m)$	$l_{M1}=l_{M2}(\mu m)$	Calc'ed(V)	Simu'ed(V)	Error(%)
3.00	6	1.8	24	-1	-1	0
4.35	7.8	1.8	24	-1.5	-1.45	3.3
5.94	10.8	1.8	24	-2	-1.95	2.5
7.78	18.6	2.4	24	-2.5	-2.5	0
9.86	18	1.8	24	-3	-2.9	3.3
12.20	25.2	1.8	24	-3.5	-3.4	3

Table 6. Comparison of Calculated and Simulated Results of Two P Transistor Divider Negative Voltage Generator

Table 6 is a comparison of calculated and simulated negative voltages. Similar to the CMOS divider circuit, the calculated and simulated results are close to within a few percentage points. The error source is mainly the round off of the transistor sizes.

So far we have shown that we can generate both regulated substrate bias with CMOS divider circuit, as well as the more negative voltage with Two P-Transistor divider circuit. The following will demonstrate the generation of current source utilizing the two circuits. Since the current is basically generated the same way as the free-run circuit in the last section, we can set the CMOS divider circuit to generate the substrate bias V_{BB} of -1.5V and the Two P-transistor circuit to generate a more negative voltage V_{neg} of -3.5V. Like generating the current source with the free run circuits, we can have a table similar to Table 1. Here the current source transistor is configured the same way with its body n-well grounded. The cathode voltage of the guard ring diode is about $-1.5V - 0.4V = -1.9V$. So we have: $V_{SB} = -1.9V$.

From equation (6) we can calculate the V_{tp} here as

$$V_{tp} = 1.2243V \quad (23)$$

And from equation (7), with $k_p = 2.5454E-5$, $V_{sg} = -1.9 - (-3.5) = 1.6V$, we can generate the following table for the current source transistor:

$I_{bias}(\mu A)$	Possible Transistor Sizes(μm)	
	w	l
2	6.6	6
4	6.6	3
6	19.8	6
8	13.2	3
10	6.6	1.2
12	12	1.8
14	18.6	2.4
16	10.8	1.2
18	12	1.2
20	13.2	1.2

Table 7. Calculated Transistor Sizes for Current Source Using Feedback Loop Regulated Circuits

Simulations were performed and the results are very close to the calculated ones. Table 8 shows the comparison of calculated and simulated results. Comparing it to the results of the non-regulated circuit, we can see that this current source generator provides much better results. The current source generator using free run charge pump circuits has an over 50% difference between calculated and simulated results. The current source here is giving us a much more practical means to predict the outcome.

Transistor Sizes(μm)		Current(μA)		error(%)
w	l	Calculated	Simulated	
6.6	6	2	2.1	5
6.6	3	4	4.1	2.5
19.8	6	6	6	0
13.2	3	8	8.1	1.25
6.6	1.2	10	10.2	2
12	1.8	12	12.5	2
18.6	2.4	14	13.8	1.4
10.8	1.2	16	15.5	3.1
12	1.2	18	18.5	2.8
13.3	1.2	20	20.2	1

Table 8. Comparison of Calculated and Simulated Results of Current Source Generator Using Feedback Loop Regulated Circuits.

Figure 23 is the simulated transient response of this current source generator when the current source transistor is set to generate $4\mu\text{A}$. The first part of the graph shows the current generated which at steady state is a little over $4\mu\text{A}$. The second part is the substrate bias generated with the CMOS divider circuit which is very close to the desired -1.5V . The third graph illustrates the V_{neg} generated with the Two P-transistor divider circuit at about -3.5V . The simulation used both C_{sub} for the substrate bias generator and the off-chip capacitor at the V_{neg} node of 100pF . In reality both capacitors can be much larger; therefore the ripple can be further reduced.

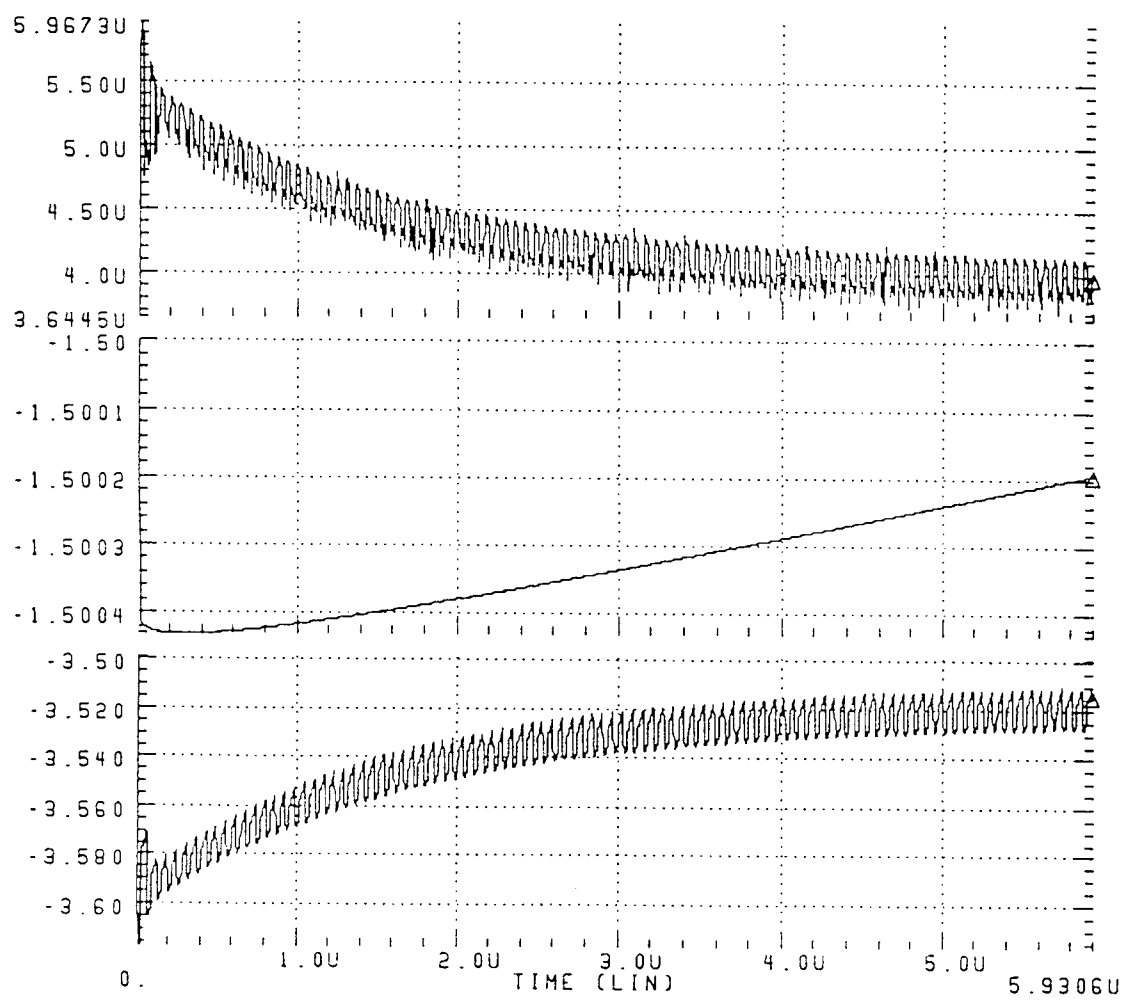


Figure 23. A Simulated Current Generated with Feedback Loop Regulated Circuits.

5. CONCLUSION

This project focuses on the on-chip generation of negative voltages and current sources for guard ring diodes. Two different types of circuits are proposed and simulated for generating the negative voltages in CMOS technology.

The first approach is a non-regulated circuit where the output voltage is determined by VDD, load resistance, charge pump capacitance, and oscillating frequency. This voltage cannot be controlled and varies from chip to chip depending upon the substrate leakage current. To regulate this voltage, we used series diodes in parallel with the load. The load regulation is improved by doing so but the output voltage is limited to multiple diode drop voltage increments. This approach satisfies the need to negatively bias the substrate where the accuracy of this voltage is not critical, mostly in digital circuits. However, when it comes to generating current sources for guard ring diodes, this type of circuit becomes very inaccurate to provide desirable voltage references.

The second approach we experimented with employs a feedback loop mechanism to precisely determine the output voltage. Because the feedback parameter is the output voltage, the load current becomes irrelevant to the voltage output as long as the charge pump can sustain the current loss. In other words, the output voltage is well regulated over load. This stabilizes the negative voltage generator over process variation. Another nice thing about this circuit is that the voltage output can be programmable by having an array of voltage dividers. This should be very useful in testing the actual guard ring diode circuit.

The generation of current sources for guard ring diodes is based on the on-chip generation of the negative voltages. The fact that the anodes of the guard ring diodes are the substrates requires a more negative voltages at the cathode of the diodes in

order to forward bias them. We used the PMOS transistor current source in series with the guard ring diode. In this configuration, the accuracy of the voltages at the two ends becomes crucial. The square law I-V relationship of MOS transistor indicates that a small voltage change results in a much larger current. Of the two forms of negative voltage generators we experimented with, the feedback loop regulated circuits have obvious advantages over the unregulated circuits. The simulation results show that the former will generate a current accurate to within a few percents from the calculated value while the latter has over a 50% error.

This project has been conducted mostly to support thw work on 'Forward Biased Guard Ring Diodes for Suppression of Substrate Noise in Mixed-Mode CMOS Circuits'. Future work should include an automatic biasing current adjustment over various substrate noise spectra.

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APPENDIX

HSPICE SOURCE FILES

*FIGURE 8

*NEGATIVE VOLTAGE GENERATED WITHOUT FEEDBACK AND REGULATING DIODES

VDD VDD 0 DC 5V

M2 10008 RO_OUT 0 10018 N L=4.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P
 M4 10009 10008 0 10018 N L=4.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P
 M6 10010 10009 0 10018 N L=4.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P
 M8 10011 10010 0 10018 N L=4.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P
 M10 10012 10011 0 10018 N L=4.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P
 M12 10013 10012 0 10018 N L=4.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P
 M14 RO_OUT 10013 0 10018 N L=4.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

M1 10008 RO_OUT VDD VDD P L=4.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P
 M3 10009 10008 VDD VDD P L=4.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P
 M5 10010 10009 VDD VDD P L=4.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P
 M7 10011 10010 VDD VDD P L=4.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P
 M9 10012 10011 VDD VDD P L=4.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P
 M11 10013 10012 VDD VDD P L=4.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P
 M13 RO_OUT 10013 VDD VDD P L=4.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

MD1 11000 RO_OUT VDD VDD P L=1.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P
 MD3 VDRIVE 11000 VDD VDD P L=1.2U W=24U PD=54U AD=72P PS=54U AS=72P
 MD2 11000 RO_OUT 0 10018 N L=1.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P
 MD4 VDRIVE 11000 0 10018 N L=1.2U W=8.4U PD=22.8U AD=25.2P PS=22.8U AS=25.2P

MCPUMP VPUMP VDRIVE VPUMP VBB N L=60U W=60U PD=126U AD=180P PS=126U
 + AS=180P

DSUB VBB VPUMP DIODE
 DGND VPUMP 0 DIODE

CSUB VBB 0 10P
 RLOAD VBB 0 500K
 .MODEL DIODE D [LEVEL=1 IS=1.548E-12 RS=7.5 TT=20N CJO=0.03P]

.IC V(RO_OUT)=5V
 .IC V(VBB)=-3.2V

.MODEL N NMOS LEVEL=3 PHI=0.600000 TOX=2.6400E-08 XJ=0.200000U TPG=1
 + VTO=0.9573 DELTA=2.8320E+00 LD=4.9090E-08 KP=8.3843E-05
 + UO=641.0 THETA=9.4100E-02 RSH=6.8510E+01 GAMMA=0.7792
 + NSUB=3.1290E+16 NFS=1.98E+12 VMAX=1.7240E+05 ETA=1.3650E-01
 + KAPPA=3.3040E-03 CGDO=9.6315E-11 CGSO=9.6315E-11
 + CGBO=2.2662E-10 CJ=5.1113E-04 MJ=0.4670 CJSW=3.7279E-10
 + MJSW=0.286904 PB=0.800000
 * WEFF = WDRAWN - DELTA_W
 * THE SUGGESTED DELTA_W IS 2.0000E-09

```
.MODEL P PMOS LEVEL=3 PHI=0.600000 TOX=2.6400E-08 XJ=0.200000U TPG=-1
+ VTO=-0.8406 DELTA=2.9950E-01 LD=1.2370E-09 KP=2.5454E-05
+ UO=194.6 THETA=7.6950E-02 RSH=3.1440E+02 GAMMA=0.5768
+ NSUB=1.7150E+16 NFS=3.46E+12 VMAX=1.0930E+05 ETA=3.0470E-02
+ KAPPA=4.4120E+00 CGDO=2.4270E-12 CGSO=2.4270E-12
+ CGBO=2.7364E-10 CJ=3.8950E-04 MJ=0.4794 CJSW=3.8646E-10
+ MJSW=0.358053 PB=0.850000
* WEFF = WDRAWN - DELTA_W
* THE SUGGESTED DELTA_W IS 1.5850E-07

.OPTION POST
.TRAN 100N 20U
.END
```

*FIGURE 12

*NEGATIVE VOLTAGE GENERATED WITH 3 REGULATING DIODES IN SERIES

VDD VDD 0 DC 5V

M2 10008 RO_OUT 0 10018 N L=4.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P
M4 10009 10008 0 10018 N L=4.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P
M6 10010 10009 0 10018 N L=4.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P
M8 10011 10010 0 10018 N L=4.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P
M10 10012 10011 0 10018 N L=4.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P
M12 10013 10012 0 10018 N L=4.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P
M14 RO_OUT 10013 0 10018 N L=4.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

M1 10008 RO_OUT VDD VDD P L=4.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P
M3 10009 10008 VDD VDD P L=4.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P
M5 10010 10009 VDD VDD P L=4.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P
M7 10011 10010 VDD VDD P L=4.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P
M9 10012 10011 VDD VDD P L=4.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P
M11 10013 10012 VDD VDD P L=4.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P
M13 RO_OUT 10013 VDD VDD P L=4.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

MD1 11000 RO_OUT VDD VDD P L=1.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P
MD3 VDRIVE 11000 VDD VDD P L=1.2U W=24U PD=54U AD=72P PS=54U AS=72P
MD2 11000 RO_OUT 0 10018 N L=1.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P
MD4 VDRIVE 11000 0 10018 N L=1.2U W=8.4U PD=22.8U AD=25.2P PS=22.8U AS=25.2P

MCPUMP VPUMP VDRIVE VPUMP VBB N L=40U W=40U PD=86U AD=120P PS=86U
+ AS=120P

DSUB VBB VPUMP DIODE
DGND VPUMP 0 DIODE

D1 0 1 DIODE
D2 1 2 DIODE
D3 2 VBB DIODE

CSUB VBB 0 10P
RLOAD VBB 0 500K
.MODEL DIODE D [LEVEL=1 IS=1.548E-12 RS=7.5 TT=20N CJO=0.03P]

.IC V(RO_OUT)=5V
.IC V(VBB)=-1.2V

.MODEL N NMOS LEVEL=3 PHI=0.600000 TOX=2.6400E-08 XJ=0.200000U TPG=1
+ VTO=0.9573 DELTA=2.8320E+00 LD=4.9090E-08 KP=8.3843E-05
+ UO=641.0 THETA=9.4100E-02 RSH=6.8510E+01 GAMMA=0.7792
+ NSUB=3.1290E+16 NFS=1.98E+12 VMAX=1.7240E+05 ETA=1.3650E-01
+ KAPPA=3.3040E-03 CGDO=9.6315E-11 CGSO=9.6315E-11
+ CGBO=2.2662E-10 CJ=5.1113E-04 MJ=0.4670 CJSW=3.7279E-10
+ MJSW=0.286904 PB=0.800000

* W_{EFF} = W_{DRAWN} - Δ_W
 * THE SUGGESTED Δ_W IS 2.0000E-09

.MODEL P PMOS LEVEL=3 PHI=0.600000 TOX=2.6400E-08 XJ=0.200000U TPG=-1
 + VTO=-0.8406 Δ=2.9950E-01 LD=1.2370E-09 KP=2.5454E-05
 + UO=194.6 THETA=7.6950E-02 RSH=3.1440E+02 GAMMA=0.5768
 + NSUB=1.7150E+16 NFS=3.46E+12 VMAX=1.0930E+05 ETA=3.0470E-02
 + KAPPA=4.4120E+00 CGDO=2.4270E-12 CGSO=2.4270E-12
 + CGBO=2.7364E-10 CJ=3.8950E-04 MJ=0.4794 CJSW=3.8646E-10
 + MJSW=0.358053 PB=0.850000
 * W_{EFF} = W_{DRAWN} - Δ_W
 * THE SUGGESTED Δ_W IS 1.5850E-07

.OPTION POST
 .TRAN 100N 20U
 .END

*FIGURE 16

*CURRENT SOURCE GENERATOR USING BASIC PUMPING CIRCUIT

*

*

VCC VCC 0 DC 5V

M2 10008 RO_OUT 0 10018 N L=4.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

M4 10009 10008 0 10018 N L=4.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

M6 10010 10009 0 10018 N L=4.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

M8 10011 10010 0 10018 N L=4.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

M10 10012 10011 0 10018 N L=4.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

M12 10013 10012 0 10018 N L=4.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

M14 RO_OUT 10013 0 10018 N L=4.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

M1 10008 RO_OUT VCC VCC P L=4.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

M3 10009 10008 VCC VCC P L=4.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

M5 10010 10009 VCC VCC P L=4.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

M7 10011 10010 VCC VCC P L=4.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

M9 10012 10011 VCC VCC P L=4.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

M11 10013 10012 VCC VCC P L=4.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

M13 RO_OUT 10013 VCC VCC P L=4.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

MD1 11000 RO_OUT VCC VCC P L=1.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

MD3 VDRIVE 11000 VCC VCC P L=1.2U W=48U PD=54U AD=72P PS=54U AS=72P

MD2 11000 RO_OUT 0 10018 N L=1.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

MD4 VDRIVE 11000 0 10018 N L=1.2U W=16U PD=22.8U AD=25.2P PS=22.8U AS=25.2P

MCPUMP VDRIVE VPUMP VDRIVE VCC P L=60U W=60U PD=240U AD=3600P PS=240U
+ AS=3600P

MCPUMPNEG VDRIVE VPUMPNEG VDRIVE VCC P L=60U W=60U PD=240U AD=3600P
+ PS=240U AS=3600P

RLOADNEG VNEG 0 500K

RLOAD VBB 0 500K

DSUB VBB VPUMP DIODE

DGND VPUMP 0 DIODE

DNEG1 VNEG VPUMPNEG DIODE

DNEG2 VPUMPNEG 0 DIODE

DGR VBB DGR_CATH DIODE

MCUR VNEG VNEG DGR_CATH 0 P W=1.8U L=6U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

D1 0 1 DIODE

D2 1 2 DIODE

D3 2 VBB DIODE


```
CSUB VBB 0 100P
CNEG VNEG 0 100P
```

```
.MODEL DIODE D [LEVEL=1 IS=1.548E-12 RS=7.5 TT=20N CJO=0.03P]
```

```
.IC V(RO_OUT)=5V
.IC V(VBB)=-1.2V
.IC V(VNEG)=-3V
.IC I(DGR)=4U
```

```
.MODEL N NMOS LEVEL=3 PHI=0.600000 TOX=2.6400E-08 XJ=0.200000U TPG=1
+ VTO=0.9573 DELTA=2.8320E+00 LD=4.9090E-08 KP=8.3843E-05
+ UO=641.0 THETA=9.4100E-02 RSH=6.8510E+01 GAMMA=0.7792
+ NSUB=3.1290E+16 NFS=1.98E+12 VMAX=1.7240E+05 ETA=1.3650E-01
+ KAPPA=3.3040E-03 CGDO=9.6315E-11 CGSO=9.6315E-11
+ CGBO=2.2662E-10 CJ=5.1113E-04 MJ=0.4670 CJSW=3.7279E-10
+ MJSW=0.286904 PB=0.800000
* WEFF = WDRAWN - DELTA_W
* THE SUGGESTED DELTA_W IS 2.0000E-09
```

```
.MODEL P PMOS LEVEL=3 PHI=0.600000 TOX=2.6400E-08 XJ=0.200000U TPG=-1
+ VTO=-0.8406 DELTA=2.9950E-01 LD=1.2370E-09 KP=2.5454E-05
+ UO=194.6 THETA=7.6950E-02 RSH=3.1440E+02 GAMMA=0.5768
+ NSUB=1.7150E+16 NFS=3.46E+12 VMAX=1.0930E+05 ETA=3.0470E-02
+ KAPPA=4.4120E+00 CGDO=2.4270E-12 CGSO=2.4270E-12
+ CGBO=2.7364E-10 CJ=3.8950E-04 MJ=0.4794 CJSW=3.8646E-10
+ MJSW=0.358053 PB=0.850000
* WEFF = WDRAWN - DELTA_W
* THE SUGGESTED DELTA_W IS 1.5850E-07
```

```
.OPTION POST
.PLOT I(DGR)
.TRAN 200N 20U
.END*
```

*FIGURE 19

*

* PROJECT NEG_BIAS

* POWERVIEW WIRELIST CREATED WITH VERSION 5.2

* INIFILE : WSPICE.INI

* OPTIONS : -M -F -N -GCMOS_MODEL

*

* CONFIG FILE: /U3/APPS/PV/STANDARD/WSPICE.CFG

*

* LEVELS :

*

.MODEL N NMOS LEVEL=3 PHI=0.600000 TOX=2.6400E-08 XJ=0.200000U TPG=1

+ VTO=0.9573 DELTA=2.8320E+00 LD=4.9090E-08 KP=8.3843E-05

+ UO=641.0 THETA=9.4100E-02 RSH=6.8510E+01 GAMMA=0.7792

+ NSUB=3.1290E+16 NFS=1.98E+12 VMAX=1.7240E+05 ETA=1.3650E-01

+ KAPPA=3.3040E-03 CGDO=9.6315E-11 CGSO=9.6315E-11

+ CGBO=2.2662E-10 CJ=5.1113E-04 MJ=0.4670 CJSW=3.7279E-10

+ MJSW=0.286904 PB=0.800000

* WEFF = WDRAWN - DELTA_W

* THE SUGGESTED DELTA_W IS 2.0000E-09

.MODEL P PMOS LEVEL=3 PHI=0.600000 TOX=2.6400E-08 XJ=0.200000U TPG=-1

+ VTO=-0.8406 DELTA=2.9950E-01 LD=1.2370E-09 KP=2.5454E-05

+ UO=194.6 THETA=7.6950E-02 RSH=3.1440E+02 GAMMA=0.5768

+ NSUB=1.7150E+16 NFS=3.46E+12 VMAX=1.0930E+05 ETA=3.0470E-02

+ KAPPA=4.4120E+00 CGDO=2.4270E-12 CGSO=2.4270E-12

+ CGBO=2.7364E-10 CJ=3.8950E-04 MJ=0.4794 CJSW=3.8646E-10

+ MJSW=0.358053 PB=0.850000

* WEFF = WDRAWN - DELTA_W

* THE SUGGESTED DELTA_W IS 1.5850E-07

.MODEL DIODE D [LEVEL=1 IS=1.548E-12 RS=7.5 TT=20N CJO=0.03P VB=-60]

MPULLUP N1N137 N1N137 VDD VDD P L=24U W=6U PD=18U AD=18P PS=18U AS=18P

MNTHRS N1N137 0 VBB VBB N L=24U W=12.6U PD=31.2U AD=37.8P PS=31.2U AS=37.8P

M1I117 N1N135 N1N137 VDD VDD P L=1.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

MNTRSH N1N135 N1N137 0 VBB N L=1.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

M1I119 N1N133 N1N135 VDD VDD P L=1.2U W=16.2U PD=38.4U AD=48.6P PS=38.4U

AS=48.6P

M1I120 N1N133 N1N135 0 VBB N L=1.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

M1I121 N1N131 N1N133 VDD VDD P L=1.2U W=48.6U PD=103.2U AD=145.8P PS=103.2U

+ AS=145.8P

M1I122 N1N131 N1N133 0 VBB N L=1.2U W=16.2U PD=38.4U AD=48.6P PS=38.4U AS=48.6P

M1I123 ROPWR N1N131 VDD VDD P L=1.2U W=97.2U PD=200U AD=300P PS=200U AS=300P

M1I124 ROPWR N1N131 0 VBB N L=1.2U W=32.4U PD=72U AD=99P PS=72U AS=99P

M1I159 N1N160 N1N164 VDD VDD P L=1.2U W=21.6U PD=49.2U AD=64.8P PS=49.2U

AS=64.8P

M1I161 N1N164 ROOUT 0 VBB N L=1.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

M1I162 N1N164 ROOUT VDD VDD P L=1.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

M1I163 N1N160 N1N164 0 VBB N L=1.2U W=7.2U PD=20.4U AD=21.6P PS=20.4U AS=21.6P

MPUMP N1N160 N1N174 N1N160 VDD P L=60U W=60U PD=126U AD=180P PS=126U AS=180P

D1I176 VBB N1N174 DIODE
 D1I177 N1N174 0 DIODE
 C1 VBB 0 10P

M1I110 N1N14 ROOUT 0 VBB N L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P
 M1I111 N1N14 ROOUT ROPWR VDD P L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P
 M1I168 N1N70 N1N14 0 VBB N L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P
 M1I169 N1N70 N1N14 ROPWR VDD P L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P
 M1I174 N1N76 N1N70 0 VBB N L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P
 M1I175 N1N76 N1N70 ROPWR VDD P L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P
 M1I180 N1N87 N1N76 0 VBB N L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P
 M1I181 N1N87 N1N76 ROPWR VDD P L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P
 M1I188 N1N92 N1N87 ROPWR VDD P L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P
 M1I189 N1N92 N1N87 0 VBB N L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P
 M1I194 N1N93 N1N92 ROPWR VDD P L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P
 M1I195 N1N93 N1N92 0 VBB N L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P
 M1I196 ROOUT N1N93 0 VBB N L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P
 M1I197 ROOUT N1N93 ROPWR VDD P L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P

VDD VDD 0 5V

.OPTION POST
 .TRAN 1NS 5US
 .PLOT I(MNTHRS)
 .END

*FIGURE 22

*

* PROJECT NEG_BIAS

* POWERVIEW WIRELIST CREATED WITH VERSION 5.2

* INIFILE : WSPICE.INI

* OPTIONS : -M -F -N -GCMOS_MODEL

*

* CONFIG FILE: /U3/APPS/PV/STANDARD/WSPICE.CFG

*

* LEVELS :

*

.MODEL N NMOS LEVEL=3 PHI=0.600000 TOX=2.6400E-08 XJ=0.200000U TPG=1

+ VTO=0.9573 DELTA=2.8320E+00 LD=4.9090E-08 KP=8.3843E-05

+ UO=641.0 THETA=9.4100E-02 RSH=6.8510E+01 GAMMA=0.7792

+ NSUB=3.1290E+16 NFS=1.98E+12 VMAX=1.7240E+05 ETA=1.3650E-01

+ KAPPA=3.3040E-03 CGDO=9.6315E-11 CGSO=9.6315E-11

+ CGBO=2.2662E-10 CJ=5.1113E-04 MJ=0.4670 CJSW=3.7279E-10

+ MJSW=0.286904 PB=0.800000

* WEFF = WDRAWN - DELTA_W

* THE SUGGESTED DELTA_W IS 2.0000E-09

.MODEL P PMOS LEVEL=3 PHI=0.600000 TOX=2.6400E-08 XJ=0.200000U TPG=-1

+ VTO=-0.8406 DELTA=2.9950E-01 LD=1.2370E-09 KP=2.5454E-05

+ UO=194.6 THETA=7.6950E-02 RSH=3.1440E+02 GAMMA=0.5768

+ NSUB=1.7150E+16 NFS=3.46E+12 VMAX=1.0930E+05 ETA=3.0470E-02

+ KAPPA=4.4120E+00 CGDO=2.4270E-12 CGSO=2.4270E-12

+ CGBO=2.7364E-10 CJ=3.8950E-04 MJ=0.4794 CJSW=3.8646E-10

+ MJSW=0.358053 PB=0.850000

* WEFF = WDRAWN - DELTA_W

* THE SUGGESTED DELTA_W IS 1.5850E-07

.MODEL DIODE D [LEVEL=1 IS=1.548E-12 RS=7.5 TT=20N CJO=0.03P VB=-60]

MPULLUP N1N137 N1N137 VDD VDD P L=24U W=25.2U PD=56.4U AD=75.6P PS=56.4U
AS=75.6P

MNTHRS VNEG VNEG N1N137 VDD P L=24U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

M1I117 N1N135 N1N137 VDD VDD P L=1.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

MNTRSH N1N135 N1N137 0 VBB N L=1.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

M1I119 N1N133 N1N135 VDD VDD P L=1.2U W=16.2U PD=38.4U AD=48.6P PS=38.4U

AS=48.6P

M1I120 N1N133 N1N135 0 VBB N L=1.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

M1I121 N1N131 N1N133 VDD VDD P L=1.2U W=48.6U PD=103.2U AD=145.8P PS=103.2U

+ AS=145.8P

M1I122 N1N131 N1N133 0 VBB N L=1.2U W=16.2U PD=38.4U AD=48.6P PS=38.4U AS=48.6P

M1I123 ROPWR N1N131 VDD VDD P L=1.2U W=97.2U PD=200U AD=300P PS=200U AS=300P

M1I124 ROPWR N1N131 0 VBB N L=1.2U W=32.4U PD=72U AD=99P PS=72U AS=99P

M1I159 N1N160 N1N164 VDD VDD P L=1.2U W=21.6U PD=49.2U AD=64.8P PS=49.2U

AS=64.8P

M1I161 N1N164 ROOUT 0 VBB N L=1.2U W=1.8U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

M1I162 N1N164 ROOUT VDD VDD P L=1.2U W=5.4U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

M1I163 N1N160 N1N164 0 VBB N L=1.2U W=7.2U PD=20.4U AD=21.6P PS=20.4U AS=21.6P

MPUMP N1N160 N1N174 N1N160 VDD P L=60U W=60U PD=126U AD=180P PS=126U AS=180P

D1I176 VBB N1N174 DIODE

D1I177 N1N174 0 DIODE

C1 VBB 0 10P

M1I10 N1N14 ROOUT 0 VBB N L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P

M1I11 N1N14 ROOUT ROPWR VDD P L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P

M1I68 N1N70 N1N14 0 VBB N L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P

M1I69 N1N70 N1N14 ROPWR VDD P L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P

M1I74 N1N76 N1N70 0 VBB N L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P

M1I75 N1N76 N1N70 ROPWR VDD P L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P

M1I80 N1N87 N1N76 0 VBB N L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P

M1I81 N1N87 N1N76 ROPWR VDD P L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P

M1I88 N1N92 N1N87 ROPWR VDD P L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P

M1I89 N1N92 N1N87 0 VBB N L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P

M1I94 N1N93 N1N92 ROPWR VDD P L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P

M1I95 N1N93 N1N92 0 VBB N L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P

M1I96 ROOUT N1N93 0 VBB N L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P

M1I97 ROOUT N1N93 ROPWR VDD P L=4.8U W=2.4U PD=10.8U AD=7.2P PS=10.8U AS=7.2P

VDD VDD 0 5V

.OPTION POST

.TRAN 1NS 5US

.PLOT I(MNTHRS)

.END

*FIGURE 23

*CURRENT_FB.SP

MPULLUP N1N3 N1N3 VDD VDD P W=6U L=24U PD=18U AD=18P PS=18U AS=18P

CSUB VBB 0 10P

RLOAD1 0 VBB 1000K

D2 N1N162 0 DIODE

D1 VNEG N1N162 DIODE

RLOAD2 0 VNEG 1000K

C2 VNEG 0 10P

MPUMP1 N1N161 N1N162 N1N161 VDD P W=60U L=60U PD=126U AD=180P PS=120U
AS=180P

MD14 N1N161 N1N159 0 VBB N W=8.4U L=1.2U PD=22.8U AD=25.2P PS=22.8U AS=25.2P

MD13 N1N161 N1N159 VDD VDD P W=25.2U L=1.2U PD=56.4U AD=75.6P PS=56.4U AS=75.6P

MD12 N1N159 N1N157 0 VBB N W=1.8U L=1.2U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

MD11 N1N159 N1N157 VDD VDD P W=5.4U L=1.2U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

MR34 N1N157 N1N158 0 VBB N W=1.8U L=9.6U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

MR33 N1N157 N1N158 N1N160 VDD P W=5.4U L=9.6U PD=16.8U AD=16.2P PS=16.8U AS=16.2
P

MR32 N1N158 N1N156 0 VBB N W=1.8U L=9.6U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

MR31 N1N158 N1N156 N1N160 VDD P W=5.4U L=9.6U PD=16.8U AD=16.2P PS=16.8U AS=16.2
P

MR30 N1N156 N1N152 0 VBB N W=1.8U L=9.6U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

MR29 N1N156 N1N152 N1N160 VDD P W=5.4U L=9.6U PD=16.8U AD=16.2P PS=16.8U AS=16.2
P

MR28 N1N152 N1N151 0 VBB N W=1.8U L=9.6U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

MR26 N1N151 N1N153 0 VBB N W=1.8U L=9.6U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

MR27 N1N152 N1N151 N1N160 VDD P W=1.8U L=1.2U PD=16.8U AD=16.2P PS=16.8U AS=16.2
P

MR24 N1N153 N1N155 0 VBB N W=1.8U L=9.6U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

MR25 N1N151 N1N153 N1N160 VDD P W=1.8U L=1.2U PD=16.8U AD=16.2P PS=16.8U AS=16.2
P

MR23 N1N153 N1N155 N1N160 VDD P W=1.8U L=1.2U PD=16.8U AD=16.2P PS=16.8U AS=16.2
P

MR22 N1N155 N1N157 0 VBB N W=1.8U L=9.6U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

MR21 N1N155 N1N157 N1N160 VDD P W=1.8U L=1.2U PD=16.8U AD=16.2P PS=16.8U AS=16.2
P

M18 N1N160 N1N150 0 VBB N W=30U L=9.6U PD=66U AD=90P PS=66U AS=90P

M17 N1N160 N1N150 VDD VDD P W=90U L=1.2U PD=186U AD=270P PS=186U AS=270P

M16 N1N150 N1N149 0 VBB N W=10.8U L=1.2U PD=27.6U AD=32.4P PS=27.6U AS=32.4P

M15 N1N150 N1N149 VDD VDD P W=36U L=1.2U PD=78U AD=108P PS=78U AS=108P

M14 N1N149 N1N148 0 VBB N W=5.4U L=1.2U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

M13 N1N149 N1N148 VDD VDD P W=16.2U L=1.2U PD=38.4U AD=48.6P PS=38.4U AS=48.6P

M12 N1N148 N1N147 0 VBB N W=1.8U L=1.2U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

M11 N1N148 N1N147 VDD VDD P W=5.4U L=1.2U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

MPULLDOWN1 VNEG VNEG N1N147 VDD P W=1.8U L=24U PD=9.6U AD=5.4P PS=9.6U
+ AS=5.4P

MPULLUP1 N1N147 N1N147 VDD VDD P W=24U L=24U PD=54U AD=72P PS=48U AS=72P

DGR VBB N1N166 DIODE

MCS VNEG VNEG N1N166 0 P W=6.6U L=3U PD=19.2U AD=19.8P PS=19.2U AS=19.8P

MPULLDOWN N1N3 0 VBB VBB N W=12.6U L=24U PD=31.2U AD=37.8P PS=31.2U AS=37.8P

M1 N1N10 N1N3 VDD VDD P W=5.4U L=1.2U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

M2 N1N10 N1N3 0 VBB N W=1.8U L=1.2U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

M3 N1N18 N1N10 VDD VDD P W=16.2U L=9.6U PD=39.6U AD=48.6P PS=39.6U AS=48.6P

M4 N1N18 N1N10 0 VBB N W=5.4U L=1.2U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

M5 N1N24 N1N18 VDD VDD P W=36U L=1.2U PD=78U AD=108P PS=72U AS=108P

M6 N1N24 N1N18 0 VBB N W=10.8U L=1.2U PD=27.6U AD=32.4P PS=27.6U AS=32.4P

M8 N1N31 N1N24 0 VBB N W=30U L=1.2U PD=66U AD=90P PS=66U AS=90P

M7 N1N31 N1N24 VDD VDD P W=90U L=1.2U PD=186U AD=270P PS=186U AS=270P

MR1 N1N36 N1N67 N1N31 VDD P W=5.4U L=9.6U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

MR2 N1N36 N1N67 0 VBB N W=1.8U L=9.6U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

MR4 N1N43 N1N36 0 VBB N W=1.8U L=9.6U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

MR3 N1N43 N1N36 N1N31 VDD P W=5.4U L=9.6U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

MR7 N1N48 N1N49 N1N31 VDD P W=5.4U L=9.6U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

MR8 N1N48 N1N49 0 VBB N W=1.8U L=9.6U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

MR6 N1N49 N1N43 0 VBB N W=1.8U L=9.6U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

MR5 N1N49 N1N43 N1N31 VDD P W=5.4U L=9.6U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

MR11 N1N60 N1N61 N1N31 VDD P W=5.4U L=9.6U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

MR12 N1N60 N1N61 0 VBB N W=1.8U L=9.6U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

MR14 N1N67 N1N60 0 VBB N W=1.8U L=9.6U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

MR13 N1N67 N1N60 N1N31 VDD P W=5.4U L=9.6U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

MR9 N1N61 N1N48 N1N31 VDD P W=5.4U L=9.6U PD=16.8U AD=16.2P PS=16.8U AS=16.2P

MR10 N1N61 N1N48 0 VBB N W=1.8U L=9.6U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

MD3 N1N78 N1N79 VDD VDD P W=25.2U L=1.2U PD=56.4U AD=75.6P PS=56.4U AS=75.6P

MD4 N1N78 N1N79 0 VBB N W=8.4U L=1.2U PD=22.8U AD=25.2P PS=22.8U AS=25.2P

MD2 N1N79 N1N67 0 VBB N W=1.8U L=1.2U PD=9.6U AD=5.4P PS=9.6U AS=5.4P

MD1 N1N79 N1N67 VDD VDD P W=5.4U L=1.2U PD=10.8U AD=7.2P PS=10.8U AS=7.2P

MPUMP N1N78 N1N97 N1N78 VDD P W=60U L=60U PD=126U AD=180P PS=126U AS=180P

DSUB VBB N1N97 DIODE

DGND N1N97 0 DIODE

.IC V(VBB)=-1.4V

.IC V(VNEG)=-3.5V

.IC V(N1N67)=5V

.IC V(N1N157)=5V

*.IC I(IGR)=4U

.MODEL N NMOS LEVEL=3 PHI=0.600000 TOX=2.6400E-08 XJ=0.200000U TPG=1

+ VTO=0.9573 DELTA=2.8320E+00 LD=4.9090E-08 KP=8.3843E-05

+ UO=641.0 THETA=9.4100E-02 RSH=6.8510E+01 GAMMA=0.7792

```

+ NSUB=3.1290E+16 NFS=1.98E+12 VMAX=1.7240E+05 ETA=1.3650E-01
+ KAPPA=3.3040E-03 CGDO=9.6315E-11 CGSO=9.6315E-11
+ CGBO=2.2662E-10 CJ=5.1113E-04 MJ=0.4670 CJSW=3.7279E-10
+ MJSW=0.286904 PB=0.800000
* WEFF = WDRAWN - DELTA_W
* THE SUGGESTED DELTA_W IS 2.0000E-09

```

```

.MODEL P PMOS LEVEL=3 PHI=0.600000 TOX=2.6400E-08 XJ=0.200000U TPG=-1
+ VTO=-0.8406 DELTA=2.9950E-01 LD=1.2370E-09 KP=2.5454E-05
+ UO=194.6 THETA=7.6950E-02 RSH=3.1440E+02 GAMMA=0.5768
+ NSUB=1.7150E+16 NFS=3.46E+12 VMAX=1.0930E+05 ETA=3.0470E-02
+ KAPPA=4.4120E+00 CGDO=2.4270E-12 CGSO=2.4270E-12
+ CGBO=2.7364E-10 CJ=3.8950E-04 MJ=0.4794 CJSW=3.8646E-10
+ MJSW=0.358053 PB=0.850000
* WEFF = WDRAWN - DELTA_W
* THE SUGGESTED DELTA_W IS 1.5850E-07

```

```

.MODEL DIODE D [LEVEL=1 IS=1.548E-12 RS=7.5 TT=20N CJO=0.03P VB=-60]

```

```

VDD VDD 0 5V

```

```

.OPTION POST
.TRAN 100NS 30US
.PLOT I(DGR)
.END

```